OPT8241 3D Time-of-Flight Sensor

1 Features

- Imaging Array:
  - 320 × 240 Array
  - 1/3" Optical Format
  - Pixel Pitch: 15 µm
  - Up to 150 Frames per Second
- Optical Properties:
  - Responsivity: 0.35 A/W at 850 nm
  - Demodulation Contrast: 45% at 50 MHz
  - Demodulation Frequency: 10 MHz to 100 MHz
- Output Data Format:
  - 12-Bit Phase Correlation Data
  - 4-Bit Common-Mode (Ambient)
- Chipset Interface:
  - Compatible with TI's Time-of-Flight Controller OPT9221
- Sensor Output Interface:
  - CMOS Data Interface (50-MHz DDR, 16-Lane Data, Clock and Frame Markers)
  - LVDS:
    - 600 Mbps, 3 Data Pairs
    - 1-LVDS Bit Clock Pair, 1-LVDS Sample Clock Pair
- Timing Generator (TG):
  - Addressing Engine with Programmable Region of Interest (ROI)
  - Modulation Control
  - De-Aliasing
  - Master, Slave Sync Operation
- I^2C Slave Interface for Control
- Power Supply:
  - 3.3-V I/O, Analog
  - 1.8-V Analog, Digital, I/O
  - 1.5-V Demodulation (Typical)
- Optimized Optical Package (COG-78):
  - 8.757 mm × 7.859 mm × 0.7 mm
  - Integrated Optical Band-Pass Filter (830 nm to 867 nm)
  - Optical Fiducials for Easy Alignment
- Operating Temperature: 0°C to 70°C

2 Applications

- Depth Sensing:
  - Location and Proximity Sensing
  - 3D Scanning
  - 3D Machine Vision
  - Security and Surveillance
  - Gesture Controls
  - Augmented and Virtual Reality

3 Description

The OPT8241 time-of-flight (ToF) sensor is part of the TI 3D ToF image sensor family. The device combines ToF sensing with an optimally-designed analog-to-digital converter (ADC) and a versatile, programmable timing generator (TG). The device offers quarter video graphics array (QVGA 320 x 240) resolution data at frame rates up to 150 frames per second (600 readouts per second).

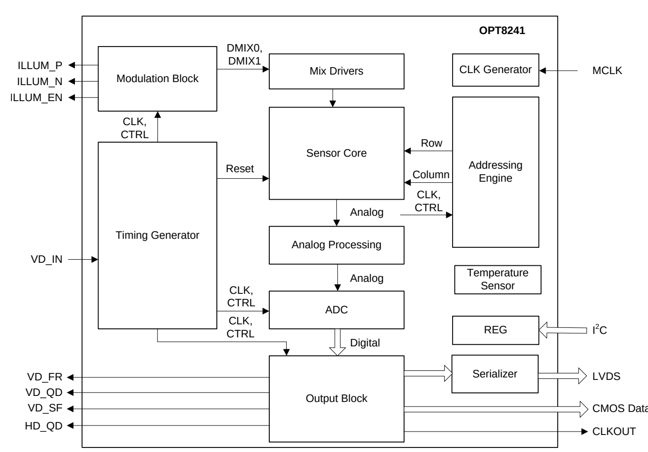
The built-in TG controls the reset, modulation, readout, and digitization sequence. The programmability of the TG offers flexibility to optimize for various depth-sensing performance metrics (such as power, motion robustness, signal-to-noise ratio, and ambient cancellation).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPT8241	COG (78)	7.859 mm × 8.757 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2015) to Revision B	Page
• Changed equations to correct format throughout document	1
• Changed name of *Function* column in *Pin Functions* table	4
• Changed SCL and SDATA pin descriptions in *Pin Functions* table	5
• Added parameter names to *Sensor* section of *Electrical Characteristics* table	7
• Changed depth resolution description in Table 5	21

Changes from Original (June 2015) to Revision A	Page
• Released to production	1

5 Pin Configuration and Functions

NBN Package
COG-78
Top View (Representative, Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	NC	GPO[0]	SDATA	GND	VMIXH	VMIXH	GND	GND	VMIXH	VMIXH	GND	ILLUM_P	ILLUM_N	DVDDH	GND	ILLUM_EN	AVDDH	AVDD_PLL	NC
B	GPO[1]		SCLK														SUB_BIAS		MCLK
C	VD_IN		RSTZ														NC		DEMOD_CLK
D	HD_QD		AVDD														RFU		TP2
E	VD_QD		AVSS														PVDD		QPORT
F	VD_FR		REFM														AVSS_PLL		IOVDD
G	IOVSS		REFP														AVDD		DVSS
H	IOVDD		AVSS														AVSS		DVDD
J	CMOS[14]		VD_SF														TP1		SUM_M
K	CMOS[13]		CMOS[15]														SUM_P		DIFF1_M
L	CMOS[12]		CMOS[11]														DIFF1_P		DCLKM
M	NC	CMOS[10]	CMOS[9]	CMOS[8]	CLKOUT	CMOS[7]	CMOS[6]	CMOS[5]	CMOS[4]	CMOS[3]	CMOS[2]	CMOS[1]	CMOS[0]	PCLK_P	PCLK_M	DIFF0_P	DIFF0_M	DCLKP	NC

Pin Functions

PIN		FUNCTION	I/O BANK	DESCRIPTION
NAME	NO.			
AVDD	D3, G17	Power	—	1.8-V analog VDD
AVDD_PLL	A18	Power	—	1.8-V PLL VDD
AVDDH	A17	Power	—	3.3-V analog VDD
AVSS	E3, H3, H17	GND	—	Analog ground
AVSS_PLL	F17	GND	—	PLL GND
CLKOUT	M5	O	IOVDD	Parallel data clock output
CMOS[0]	M13	O	IOVDD	Parallel data output bit 0
CMOS[1]	M12	O	IOVDD	Parallel data output bit 1
CMOS[2]	M11	O	IOVDD	Parallel data output bit 2
CMOS[3]	M10	O	IOVDD	Parallel data output bit 3
CMOS[4]	M9	O	IOVDD	Parallel data output bit 4
CMOS[5]	M8	O	IOVDD	Parallel data output bit 5
CMOS[6]	M7	O	IOVDD	Parallel data output bit 6
CMOS[7]	M6	O	IOVDD	Parallel data output bit 7
CMOS[8]	M4	O	IOVDD	Parallel data output bit 8
CMOS[9]	M3	O	IOVDD	Parallel data output bit 9
CMOS[10]	M2	O	IOVDD	Parallel data output bit 10
CMOS[11]	L3	O	IOVDD	Parallel data output bit 11
CMOS[12]	L1	O	IOVDD	Parallel data output bit 12
CMOS[13]	K1	O	IOVDD	Parallel data output bit 13
CMOS[14]	J1	O	IOVDD	Parallel data output bit 14
CMOS[15]	K3	O	IOVDD	Parallel data output bit 15
DCLKM	L19	O	LVDS	Negative LVDS bit clock
DCLKP	M18	O	LVDS	Positive LVDS bit clock
DEMOD_CLK	C19	I	IOVDD	Demodulation clock input (optional). This pin has a weak internal pulldown resistor.
DIFF0_M	M17	O	LVDS	Negative LVDS DIFF0 data pin
DIFF0_P	M16	O	LVDS	Positive LVDS DIFF0 data pin
DIFF1_M	K19	O	LVDS	Negative LVDS DIFF1 data pin
DIFF1_P	L17	O	LVDS	Positive LVDS DIFF1 data pin
DVDD	H19	Power	—	1.8-V digital VDD
DVDDH	A14	Power	—	3.3-V digital VDD
DVSS	G19	GND	—	Digital GND
GND	A4, A7, A8, A11, A15	GND	—	Ground
GPO[0]	A2	O	IOVDD	General-purpose output
GPO[1]	B1	O	IOVDD	General-purpose output
HD_QD	D1	O	IOVDD	Quad-frame line sync output
ILLUM_EN	A16	O	DVDDH	Illumination enable
ILLUM_N	A13	O	DVDDH	Illumination modulation signal; active low
ILLUM_P	A12	O	DVDDH	Illumination modulation signal; active high
IOVDD	H1, F19	Power	—	1.8-V to 3.3-V IOVDD
IOVSS	G1	GND	—	I/O GND
MCLK	B19	I	IOVDD	Main clock input for TG. This pin has a weak internal pulldown resistor.
NC	A1, A19, C17, M1, M19	NC	—	No connection
PCLK_M	M15	O	LVDS	Negative LVDS pixel clock

Pin Functions (continued)

PIN		FUNCTION	I/O BANK	DESCRIPTION
NAME	NO.			
PCLK_P	M14	O	LVDS	Positive LVDS pixel clock
PVDD	E17	Power	—	3.3-V pixel VDD
QPORT	E19	I/O	IOVDD	Debug port. Pullup with an external 1-kΩ resistor to IOVDD instead.
REFM	F3	Analog In	—	Connect REFM to GND
REFP	G3	Analog Out	—	ADC reference; connect a 10-nF capacitor close to REFM and REFP.
RFU	D17	RFU	—	Reserved for future use
RSTZ	C3	I	IOVDD	Sensor reset input. This pin has a weak internal pullup resistor.
SCL	B3	I	IOVDD	Clock I^2C slave interface
SDATA	A3	I/O	IOVDD	Data I^2C slave interface
SUB_BIAS	B17	Power	—	Substrate bias
SUM_M	J19	O	LVDS	Negative LVDS sum data
SUM_P	K17	O	LVDS	Positive LVDS sum data
TP1	J17	O	—	Debug pin 1, connect to a test pad on the board
TP2	D19	O	—	Debug pin 2, connect to a test pad on the board
VD_FR	F1	O	IOVDD	Frame sync output
VD_IN	C1	I	IOVDD	Frame sync input (optional)
VD_QD	E1	O	IOVDD	Quad-frame sync output
VD_SF	J3	O	—	Sub-frame sync output
VMIXH	A5, A6, A9, A10	Power	—	Mix driver power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IOVDD	Digital I/O supply	–0.3	4.0	V
AVDDH	Analog supply	–0.3	4.0	V
DVDDH	Digital I/O supply	–0.3	4.0	V
PVDD	Pixel supply	–0.3	4.0	V
AVDD	Analog supply	–0.3	2.2	V
VMIXH	Mix supply	–0.3	2.5	V
DVDD	Digital supply	–0.3	2.2	V
AVDD_PLL	PLL supply	–0.3	2.2	V
V_I	Input voltage at input pins	–0.3	VCC + 0.3(2)	V
T_J	Operating junction temperature	0	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VCC refers to the I/O bank voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IOVDD	Digital I/O supply	1.7	1.8 to 3.3	3.6	V
AVDDH	Analog supply	3.0	3.3	3.6	V
DVDDH	Digital I/O supply	3.0	3.3	3.6	V
PVDD	Pixel supply	3.0	3.3	3.6	V
AVDD	Analog supply	1.7	1.8	1.9	V
VMIXH	Mix supply	1.4	1.5	2.0	V
DVDD	Digital supply	1.7	1.8	1.9	V
AVDD_PLL	PLL supply	1.7	1.8	1.9	V
T_A	Operating ambient temperature	0		70	°C

6.4 Thermal Information

THERMAL METRIC(1)			OPT8241 NBN (COG) 78 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Without underfill	79.2	°C/W
		With underfill	41.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		18.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		51.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter		6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter		51.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		18.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All specifications at T_A = 25°C, V_{AVDDH} = 3.3 V, V_{AVDD} = 1.8 V, V_{VMIXH} = 1.5 V, V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, V_{PVDD} = 3.3 V, V_{SUB_BIAS} = 0 V, integration duty cycle = 10%, system clock frequency = 48 MHz, modulation frequency = 50 MHz, and 850 nm illumination, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SENSOR						
V	Maximum rows				240	Rows
H	Maximum columns				320	Columns
P_P	Pixel pitch			15		µm
POWER (Normal Operation)						
I_{AVDD_PLL}	PLL supply current			9		mA
I_{AVDD}	Analog supply current	Without dynamic power-down		40		mA
		With dynamic power-down		20		
I_{DVDDH}	3.3-V digital supply current			5		mA
I_{AVDDH}	3.3-V analog supply current	Without dynamic power-down		17		mA
		With dynamic power-down		7		
I_{PVDD}	Pixel VDD current			2		mA
I_{VMIXH}	Demodulation current	10% integration duty cycle		70		mA
		100% integration duty cycle		600		
I_{IOVDD}	I/O supply current (CMOS mode)			20		mA
	I/O supply current (LVDS mode)			2		
I_{DVDD}	Digital supply current			45		mA
POWER (Standby)						
I_{IOVDD}	I/O supply current			0.7		mA
I_{AVDD_PLL}	PLL supply current			0.3		mA
I_{AVDD}	Analog supply current			0.3		mA
I_{DVDD}	Digital supply current			0.6		mA
I_{DVDDH}	3.3-V digital supply current			1.1		mA
I_{AVDDH}	3.3-V analog supply current			0.2		mA
I_{VMIXH}	Demodulation current			0		mA
I_{PVDD}	Pixel VDD current			0		mA

Electrical Characteristics (continued)

All specifications at T_A = 25°C, V_{AVDDH} = 3.3 V, V_{AVDD} = 1.8 V, V_{VMIXH} = 1.5 V, V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, V_{PVDD} = 3.3 V, V_{SUB_BIAS} = 0 V, integration duty cycle = 10%, system clock frequency = 48 MHz, modulation frequency = 50 MHz, and 850 nm illumination, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS I/Os						
V_{IH}	Input high-level threshold				0.7 × VCC(1)	V
V_{IL}	Input low-level threshold		0.3 × VCC(1)			V
V_{OH}	Output high level	I_{OH} = –2 mA	VCC(1) – 0.45			V
		I_{OH} = –8 mA	VCC(1) – 0.5			
V_{OL}	Output Low Level	I_{OL} = 2 mA			0.35	V
		I_{OL} = 8 mA			0.65	
I_I	Input pin leakage current	Pins with pullup, pulldown resistor			±50	µA
		Pins without pullup, pulldown resistor			±10	
C_I	Input capacitance				5	pF
I_{OH}	Output current				10	mA
I_{OL}					10	

(1) VCC is equal to IOVDD or DVDDH, based on the I/O bank listed in the *Pin Functions* table.

6.6 Timing Requirements

	MIN	NOM	MAX	UNIT
MCLK duty cycle	48%		52%	
MCLK frequency	12		50	MHz
VD_IN pulse duration		2 × MCLK period		ns
RTSZ low pulse duration (reset)			100	ns

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted); V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, and V_{IOVDD} = 1.8 V

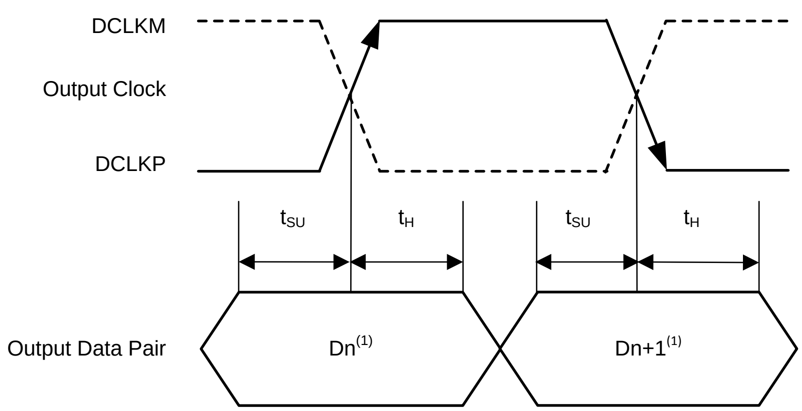
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DDR LVDS MODE						
t_{SU}	Data setup time	Data valid to zero crossing of DCLKP, DCLKM		0.48		ns
t_H	Data hold time	Zero crossing of DCLKP, DCLKM to data becoming invalid		0.54		ns
t_{FALL}, t_{RISE}	Data fall time, data rise time	Rise time measured from –100 mV to +100 mV		0.35		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time measured from –100 mV to +100 mV		0.35		ns
PARALLEL CMOS MODE						
t_{SU}	Data setup time	Data valid to zero crossing of CLKOUT		1.5		ns
t_H	Data hold time	Zero crossing of CLKOUT to data becoming invalid		3.5		ns
t_{FALL}, t_{RISE}	Data fall time, data rise time	Rise time measured from 30% to 70% of IOVDD		2.5		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time measured from 30% to 70% of IOVDD		2.2		ns

6.8 Optical Characteristics

over operating free-air temperature range (unless otherwise noted)

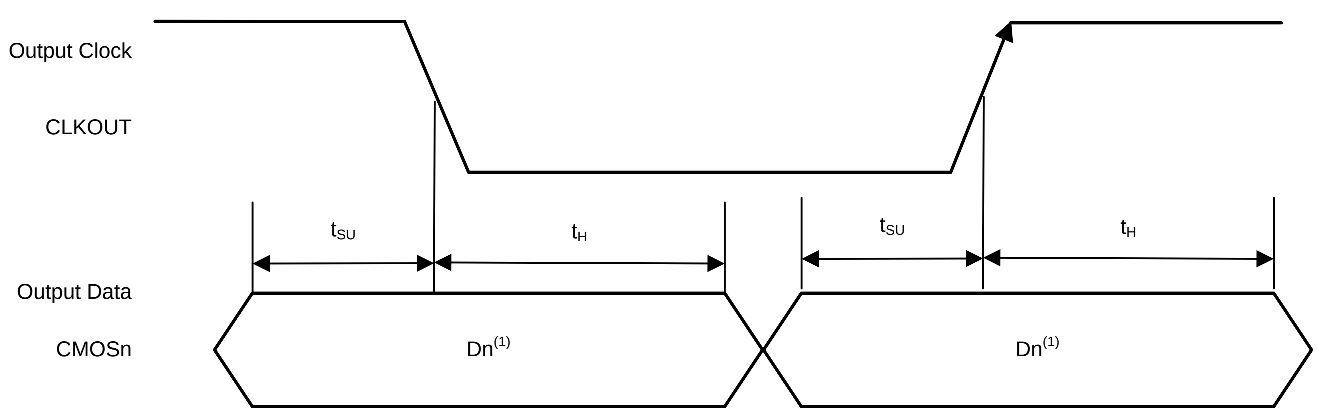
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Glass side			Top		Side
	Passband (50% relative transmittance[1])	0° incident angle		813 to 893		nm
		30° incident angle		798 to 877		nm
	Passband (90% relative transmittance[1])	0° incident angle		830 to 881		nm
		30° incident angle		838 to 867		nm
AOI	Recommended angle of incidence		0		35	Degrees
	Maximum absolute transmittance	0° incident angle		87.34% at 863		nm
		30° incident angle		81.89% at 855		nm

(1) Relative transmittance is a ratio of transmittance to maximum absolute transmittance at the same angle of incidence.



(1) Dn = bits D0, D2, D4, and so forth. Dn+1 = bits D1, D3, D5, and so forth.

Figure 1. LVDS Switching Diagram

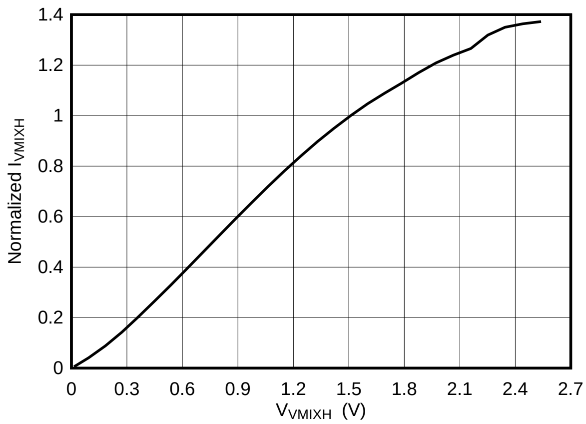


(2) Dn = bits D0, D1, D2, and so forth.

Figure 2. CMOS Switching Diagram

6.9 Typical Characteristics

At V_{AVDDH} = 3.3 V, V_{AVDD} = 1.8 V, V_{VMIXH} = 1.5 V, V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, V_{PVDD} = 3.3 V, V_{SUB_BIAS} = 0 V, and integration duty cycle = 10%, unless otherwise noted.



Normalized to V_{MIXH} = 1.5 V

Figure 3. Normalized V_{MIXH} Supply Current vs V_{MIXH} Supply Voltage

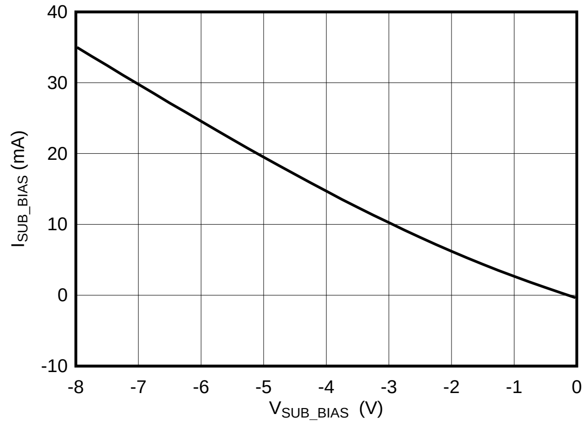


Figure 4. V_{SUB_BIAS} Supply Current vs V_{SUB_BIAS} Supply Voltage

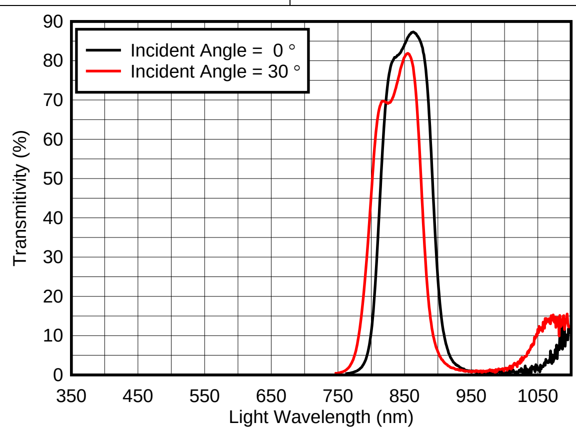


Figure 5. Optical Filter Transitivity vs Light Wavelength

7 Detailed Description

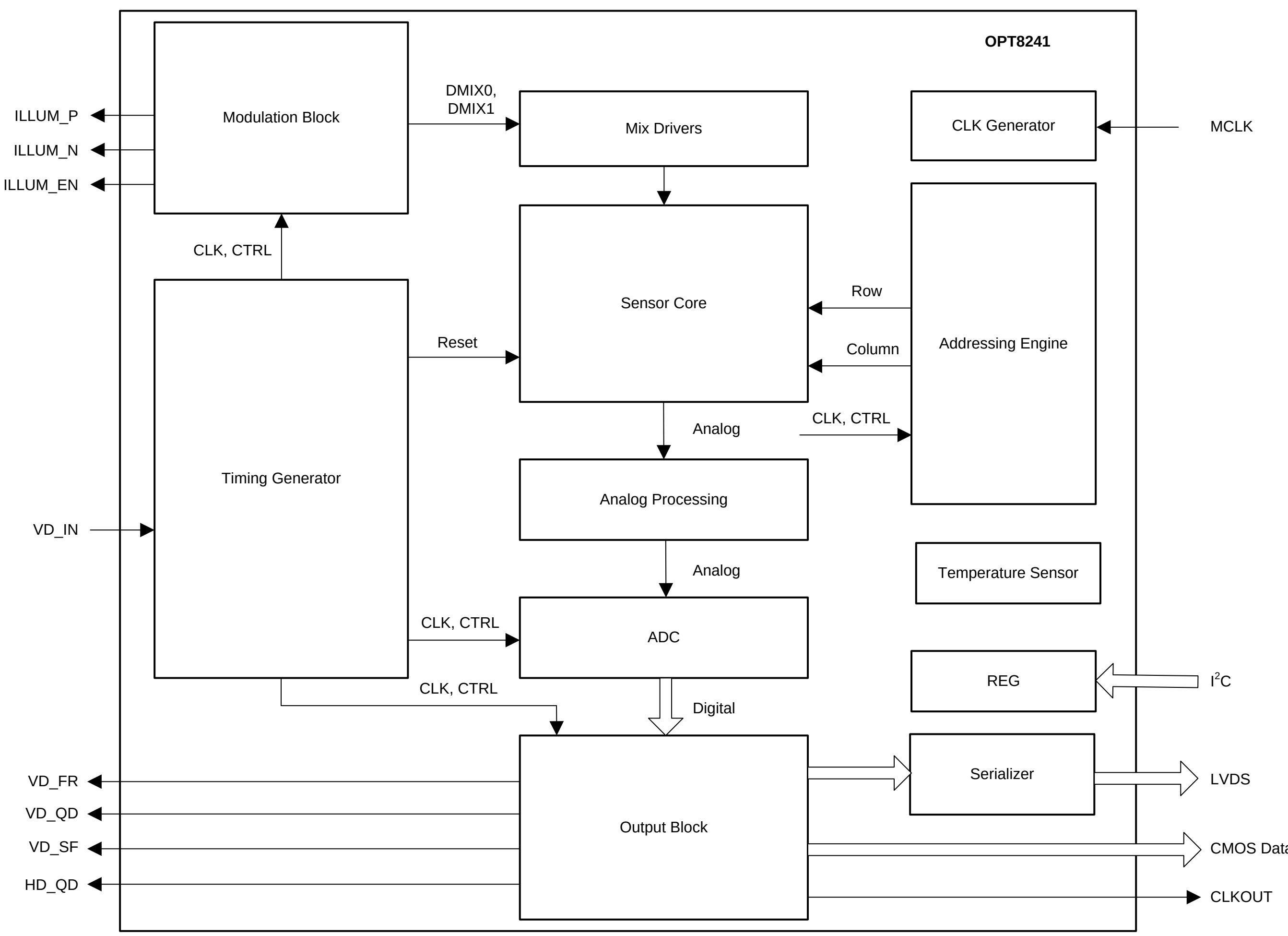
7.1 Overview

The OPT8241 is a high-performance quarter video graphics array (QVGA) resolution, 3D sensor device that senses depth information based on the time of flight (ToF) technique. The OPT8241 has a CMOS image sensor core with an integrated analog-to-digital converter (ADC), an addressing engine for the sensor core, an low-voltage differential signaling (LVDS) serializer, and an I^2C slave device. The device supports configurable timings to optimize power and performance.

The OPT8241 includes the following blocks:

- Timing generator (TG)
- Sensor core
- Addressing engine
- ADC and overload detection
- Modulation block
- Output block
- Temperature sensor
- I^2C control interface

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Block

The output block provides the output data, clock, and frame boundary signals. The positions of the following frame boundary marker signals are programmable. Table 1 lists signals that can be used by the host processor to reconstruct the frame.

Table 1. Output Frame Marker Signals

SIGNAL	TYPE	DESCRIPTION
VD_FR	Output	Frame sync
VD_SF	Output	Sub-frame sync
VD_QD	Output	Quad sync
HD_QD	Output	Row sync

7.3.1.1 Serializer and LVDS Output Interface

The sensor has an option for a serial LVDS interface. The digitized data from the ADCs are serialized and sent on three LVDS data pairs and one LVDS pixel clock pair. The DIFF0, DIFF1 pairs provide the differential data (A-B). The differential data for each pixel is 12 bits long. The pixel clock pair is 0 for the first six data bits and 1 for the next six data bits. The pixel clock can be used by the external host to identify the boundary of the 12-bit data for each pixel. The LVDS waveforms are shown in Figure 6.

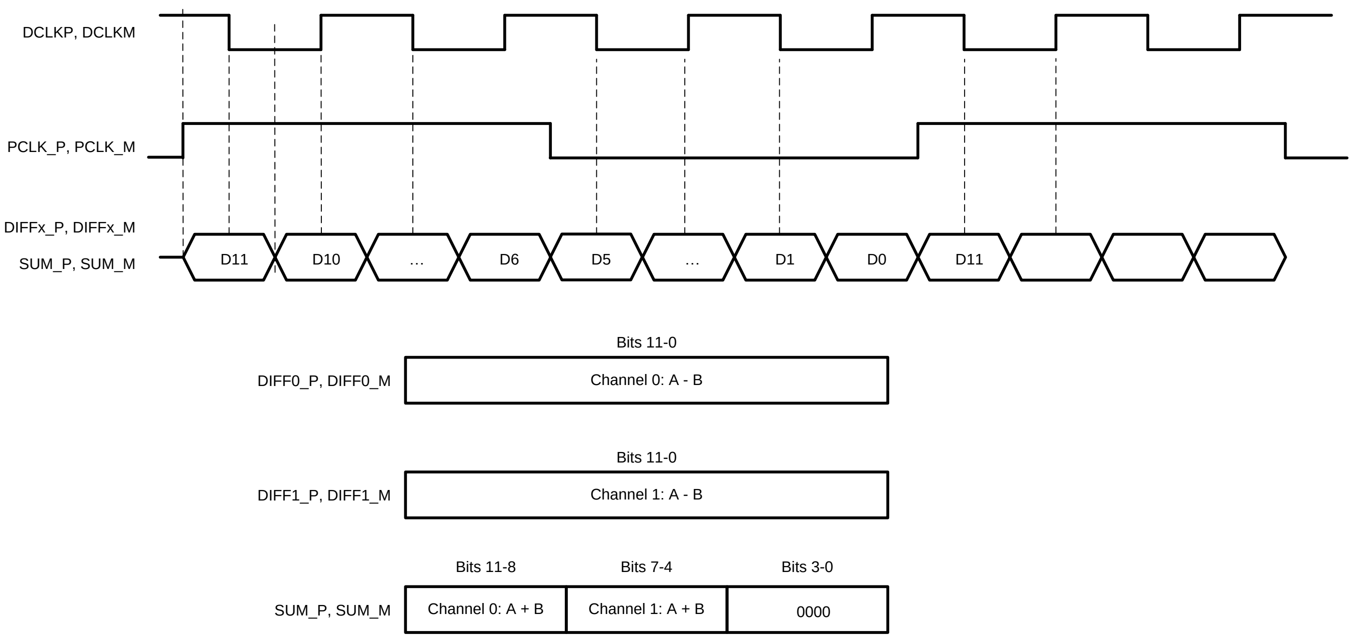


Figure 6. LVDS Output Waveforms

7.3.1.2 Parallel CMOS Output Interface

The sensor has options for both serial and parallel data output interfaces. The output data on the parallel CMOS interface toggles on both edges of the clock (DDR rate) with the output clock frequency being equal to the system clock frequency. The CMOS parallel data waveforms are shown in Figure 7.

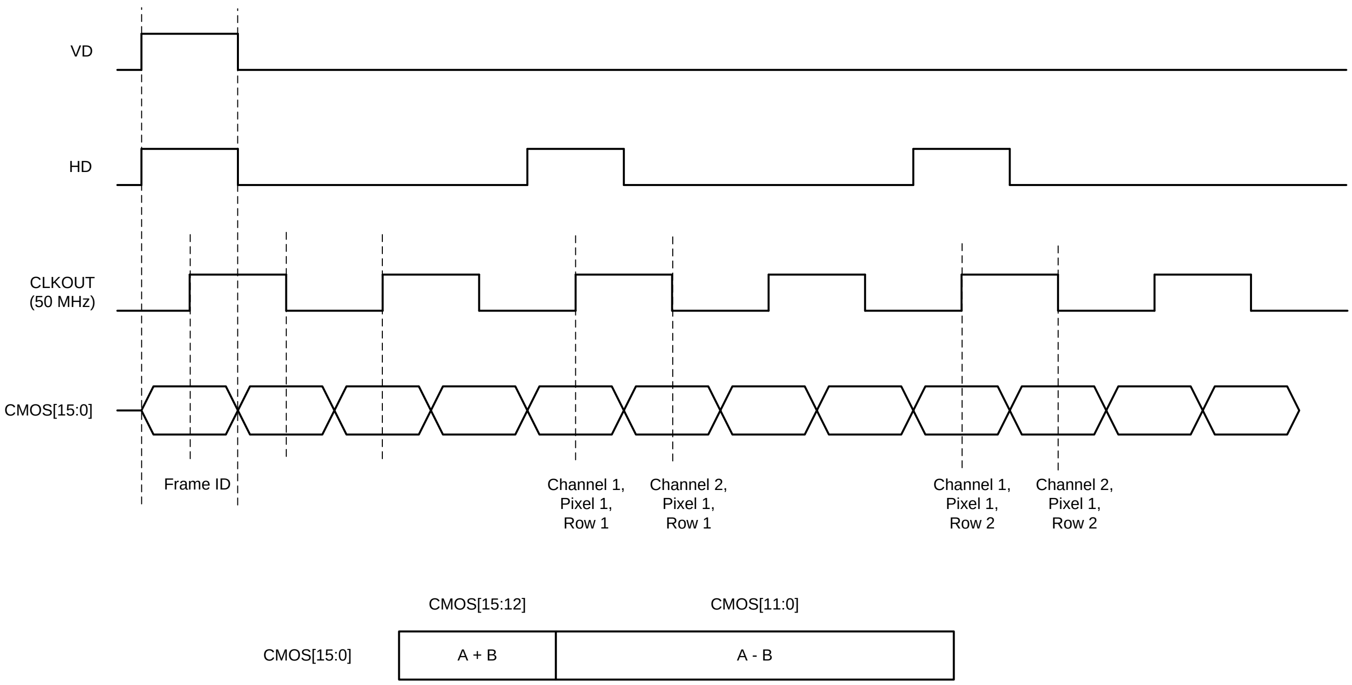


Figure 7. CMOS Output waveforms

Following the VD start, the first sample set is a frame ID that denotes the quadrant (quad) number. The frame ID format is given in Table 2.

Table 2. Frame ID Word Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	1	SF[3:0]				Q[3:0]			

Note that Q[3:0] is the quad number and SF[3:0] denotes the sub-frame number.

7.3.2 Temperature Sensor

The on-die temperature sensor can measure temperatures in the range of –25°C to 125°C. The temperature is updated every 3 ms. The temperature value is stored in a register that can be read through the I^2C interface.

7.4 Device Functional Modes

All OPT8241 control commands are directed through the OPT9221 time-of-flight controller. For more details on the functional modes of the chipset, see the OPT9221 datasheet.

7.5 Programming

The device registers are programmed by the OPT9221 time-of-flight controller. Therefore, in a typical system, the I^2C interface is connected to the OPT9221 sensor control I^2C bus; see the OPT9221 datasheet for more details.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

ToF cameras provide the complete depth map of a scene. In contrast with the scanning type light detection and ranging (LIDAR) systems, the depth map of the entire scene is captured at the same instant with an array of ToF pixels. A broad classification of applications for a 3D camera include:

- Presence detection,
- Object location,
- Movement detection, and
- 3D scanning.

The OPT8241 ToF sensor, along with TI's OPT9221 ToF controller, forms a two-chip solution for creating a 3D camera. The block diagram of a complete 3D ToF camera implementation using the OPT8241 is shown in Figure 8.

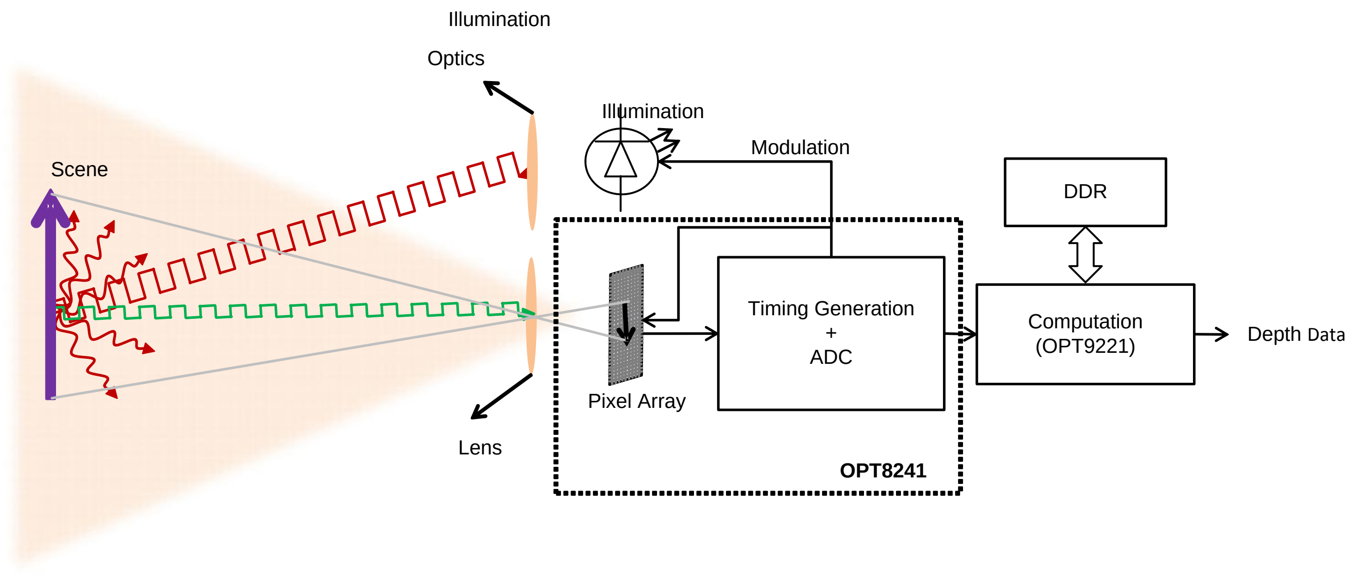


Figure 8. 3D ToF Camera

The TI ToF estimator tool can be used to estimate the performance of a ToF camera with various configurations. The estimator allows control of the following parameters:

- Depth resolution
- 2D resolution (number of pixels)
- Distance range
- Frame rate
- Field of view (FoV)
- Ambient light (in watts × nm × m^2 around the sensor filter bandwidth)
- Reflectivity of the objects

For more details on how to choose the above parameters, see the white paper on the ToF system design.

8.2 Typical Applications

8.2.1 Presence Detection for Industrial Safety

Processing 3D information and a separate foreground from the background is computationally less intensive when compared to using color information from a reg, green, blue (RGB) camera. 3D information can also be used to extract the form of the object and classify the object detected as being a human, robot, vehicle, and so forth, as shown in Figure 9.

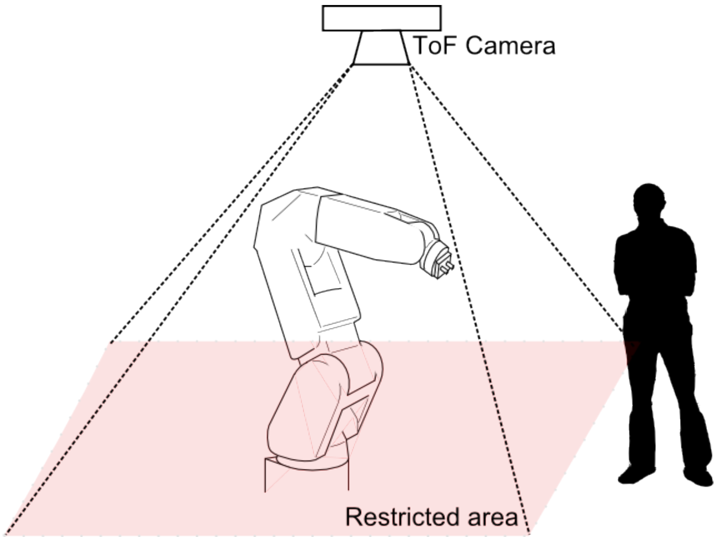


Figure 9. Industrial Safety

8.2.1.1 Design Requirements

Table 3. Industrial Safety Requirements

SPECIFICATION	VALUE	UNITS	COMMENTS
Depth resolution	7.5	Percentage of distance	Temporal standard deviation of measured distance without the use of any software filters
Frame rate	30	Frames per second	For reactions fast enough to trigger a machine shut down
Field of view	74.4 × 59.3	Degrees (H × V)	Example only, requirements may vary
Minimum distance	1	Meters	Example only, requirements may vary
Maximum distance	5	Meters	Example only, requirements may vary
Minimum reflectivity of objects at which the depth resolution is specified	40	Percentage	Assuming Lambertian reflection
Number of pixels	320 × 240	Rows x columns	Using a full array
Ambient light	0.1	W × nm × m^2 around 850 nm	Low-intensity diffused sunlight
Illumination source	Laser	—	Laser + diffuser for diffusing light uniformly through the scene

8.2.1.2 Detailed Design Procedure

Using the TI ToF estimator tool, the ToF camera design requirements can be input and the power numbers required for achieving the desired specifications can be obtained. The choice of inputs to the estimator tool is explained in the following section.

8.2.1.2.1 Frequencies of Operation

The frequencies of operation are limited by the sensor bandwidth because the illumination source is a laser. Frequencies around 75 MHz can be used to obtain a good demodulation figure of merit. Two frequencies are used to implement de-aliasing and extend the unambiguous range because frequencies around 75 MHz provide a very short unambiguous range. The two frequencies chosen for de-aliasing are 70 MHz and 80 MHz. The unambiguous range is now given by Equation 1.

$$\text{Unambiguous Range} = \frac{C}{2 \times \text{GCD}(f_1, f_2)} = \frac{299792458.0\ \text{ms}}{2 \times \text{GCD}(70\ \text{MHz}, 80\ \text{MHz})} = 14.990\ \text{m} \quad (1)$$

For the purpose of power requirement calculations, the average frequency of 75 MHz can be used in the estimator tool.

8.2.1.2.2 Number of Sub-Frames and Quads

In this example, two sub-frames and six quads are used to obtain good dynamic range and account for wide ranges of reflectivity and distance. Also, six quads (minimum) are required for implementing de-aliasing. A depth resolution of 5% instead of the requirement of 7.5% is used as the resolution input to the estimator tool to allow for margins resulting from the additional noise when using de-aliasing.

8.2.1.2.3 Field of View (FoV)

Field of view in the horizontal direction is 74.4 degrees. The diagonal FoV can be calculated using Equation 2.

$$\text{FoV}(\text{Diagonal}) = 2 \times \tan^{-1}\left[\frac{5}{4} \times \tan\left(\frac{74.4}{2}\right)\right] \approx 87° \quad (2)$$

The ratio of 5/4 is used to represent the ratio of the diagonal length to the horizontal length of the sensor.

8.2.1.2.4 Lens

A lens with a 1/3” image circle must be chosen. The FoV of the lens must match the requirements (that is, the FoV must be equal to 87 degrees, as calculated in Equation 2). A lower f.no is always better. For this example, use an f.no of 1.2.

8.2.1.2.5 Integration Duty Cycle

An integration duty cycle of less than 50% is chosen to keep the sensor cool in an industrial housing with no airflow. Choosing an even lower integration duty cycle can result in a marked increase in the peak illumination power. Higher peak illumination power results in a higher number of illumination elements and, thus, an increase in system cost.

8.2.1.2.6 Design Summary

A screen shot of the system estimator tool is shown in Figure 10.

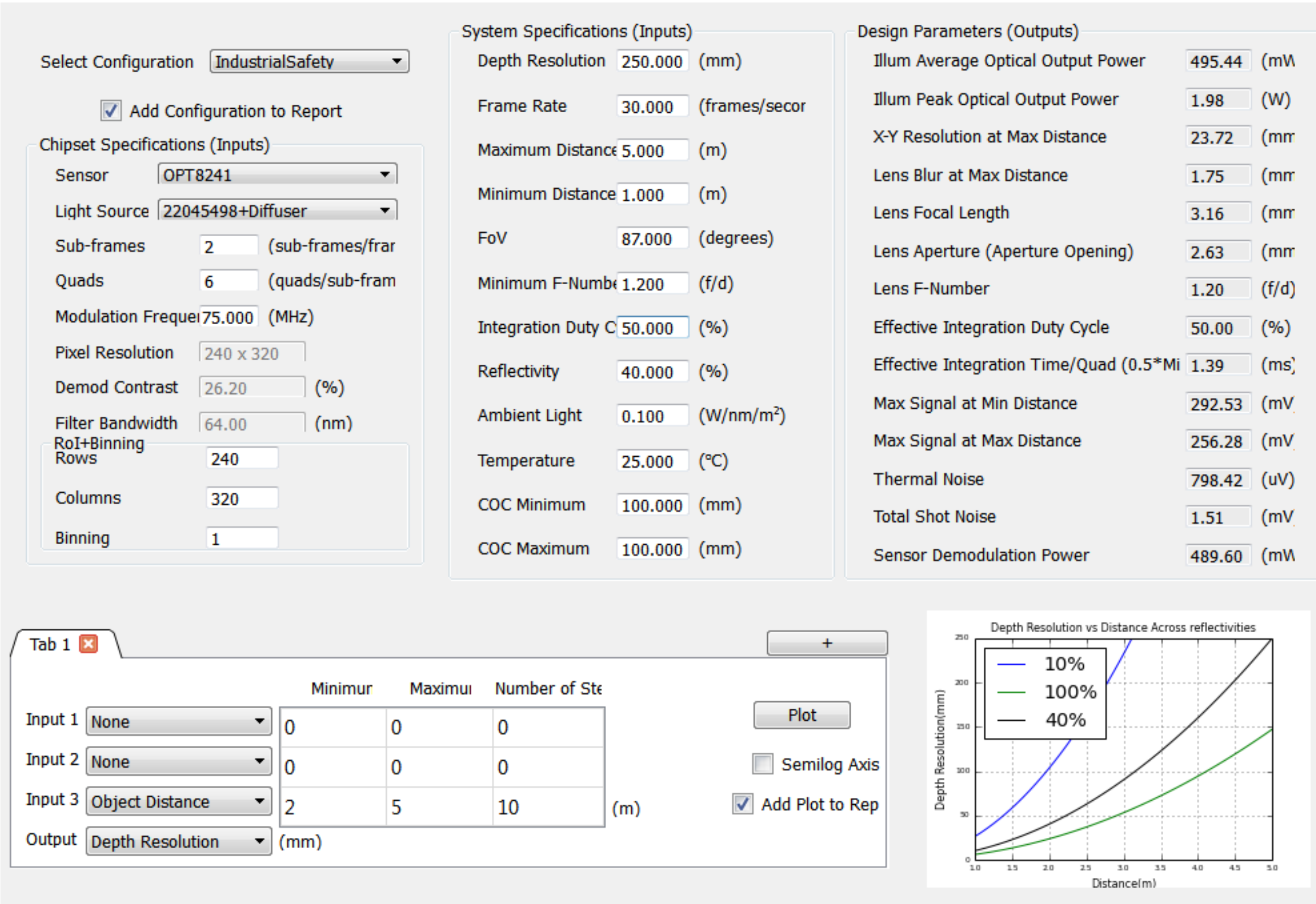
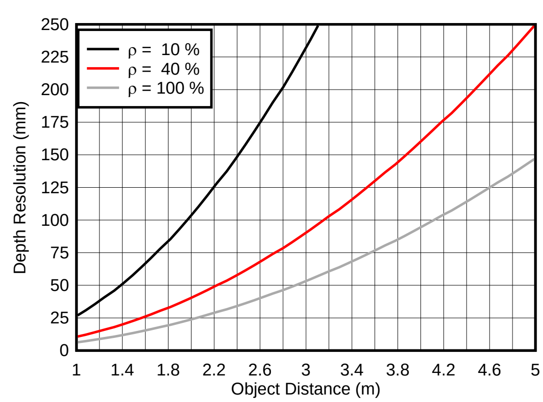


Figure 10. Screen Shot of the Estimator Tool

The illumination peak optical power of 1.98 W can be supplied using one high-power laser.

8.2.1.3 Application Curve



ρ represents object reflectivity

Figure 11. Example Industrial Safety Object Distance vs Depth Resolution

8.2.2 People Counting and Locating

Locating and tracking people is a complex problem to solve using regular RGB cameras. With the additional information of distance to each point in the scene, the algorithmic challenges become more surmountable, as shown in Figure 9.

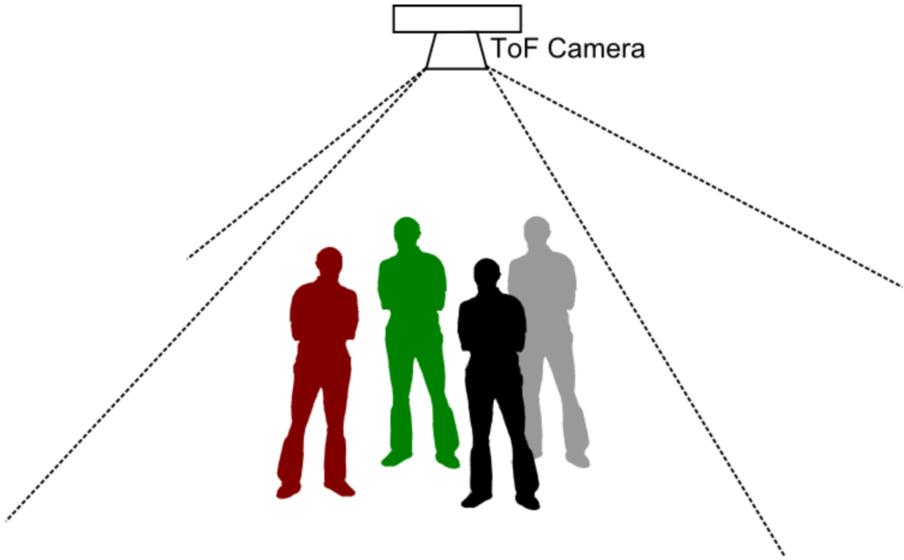


Figure 12. People Counting

8.2.2.1 Design Requirements

Table 4. People Counting Requirements

SPECIFICATION	VALUE	UNITS	COMMENTS
Depth resolution	200	mm	For basic identification of shapes
Frame rate	15	Frames per second	Reasonable update rate for moderate object movement speeds
Field of view	100.0 × 83.6	Degrees (H × V)	Higher FoVs are better for more coverage but are worse from a power requirement point of view
Minimum distance	1	Meters	Example only, requirements may vary
Maximum distance	6	Meters	Example only, requirements may vary
Typical reflectivity of objects	40	Percentage	Assuming objects reflect very little infrared light and assuming Lambertian reflection.
Number of pixels	320 × 240	Rows × columns	Using a full array
Ambient light	0	W × nm × m^2 around 850 nm	Indoor lighting conditions
Illumination source	LED	—	LED + lens optics

8.2.2.2 *Detailed Design Procedure*

Using the TI ToF estimator tool, the ToF camera design requirements can be input and the power numbers required for achieving the desired specifications can be obtained by following the procedures discussed in this section.

8.2.2.2.1 Frequencies of Operation

The frequencies of operation are limited by the LED bandwidth because the source of illumination is an LED. Frequencies around 24 MHz can be used to obtain a good demodulation figure of merit if a fast-switching infrared (IR) LED is used. The unambiguous range is given by Equation 3.

$$\text{Unambiguous Range} = \frac{C}{2 \times f} = \frac{299792458.0\ \text{ms}}{2 \times 24\ \text{MHz}} = 6.246\ \text{m} \tag{3}$$

8.2.2.2.2 Number of Sub-Frames and Quads

In this example, one sub-frame and four quads are used to minimize the effects of the sensor reset noise.

8.2.2.2.3 Field of View (FoV)

Field of view in the horizontal direction is 74.4 degrees. The diagonal field of view can be calculated using Equation 2.

$$\text{FoV}(\text{Diagonal}) = 2 \times \tan^{-1}\left[\frac{5}{4} \times \tan\left(\frac{100.0}{2}\right)\right] \approx 112.3° \tag{4}$$

The ratio of 5/4 is used to represent the ratio of the diagonal length to the horizontal length of the sensor.

8.2.2.2.4 Lens

A lens with a 1/3” image circle must be chosen. The field of view of the lens must match the requirements (that is, the FoV must be equal to 112.3 degrees, as calculated in Equation 4). A lower f.no is always better. For this example, use an f.no of 1.2.

8.2.2.2.5 Integration Duty Cycle

An integration duty cycle of 60% is chosen to keep the peak illumination power requirements low. Higher peak illumination power results in a higher number of illumination elements and, thus, an increase in system cost.

8.2.2.2.6 Design Summary

A screen shot of the system estimator tool is shown in Figure 13.

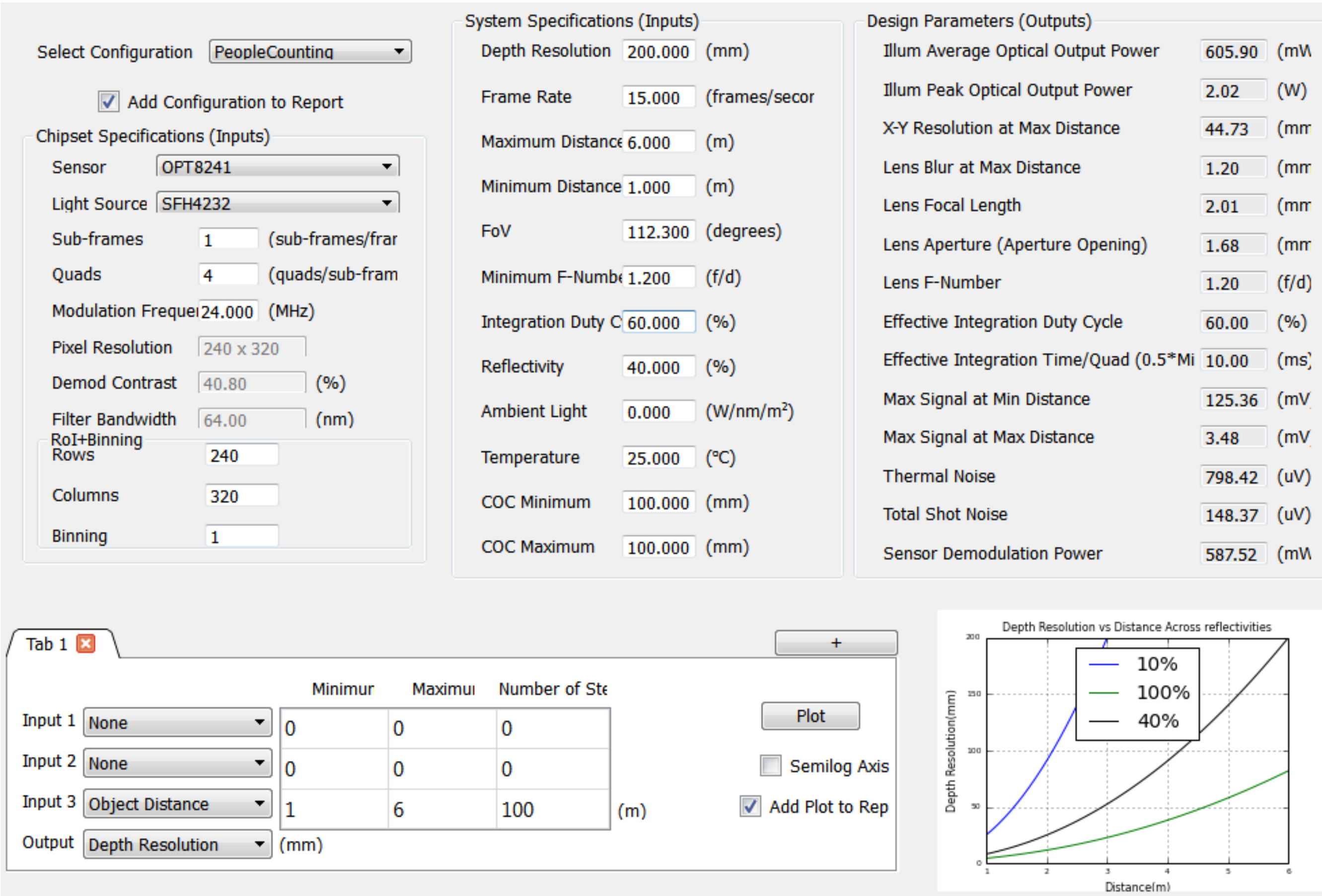
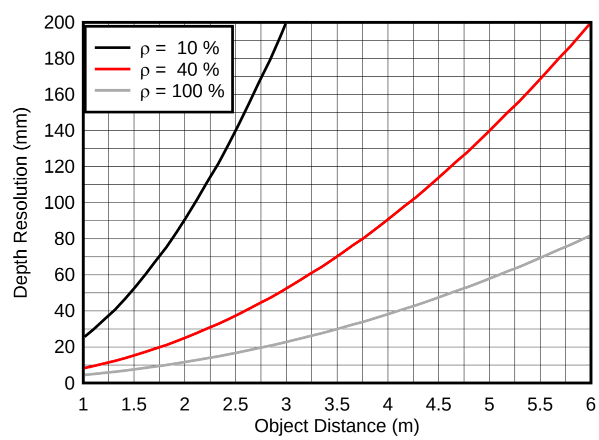


Figure 13. Screen Shot of the Estimator Tool

The illumination peak optical power of 2.0 W can be supplied using a single high-power LED.

8.2.2.3 Application Curve



ρ represents object reflectivity

Figure 14. Example People-Counting Object Distance vs Depth Resolution

8.2.3 People Locating and Identification

A skeletal structure can be used to classify identified shapes (such as humans, machines, pets, and so forth). Other possibilities include classification of people (such as children and elderly). Even identification of humans by matching the shape and movement to an existing database is possible. Such information can lend itself for use in a variety of retail solutions, home safety, security, and public and private surveillance systems, as shown in Figure 15.

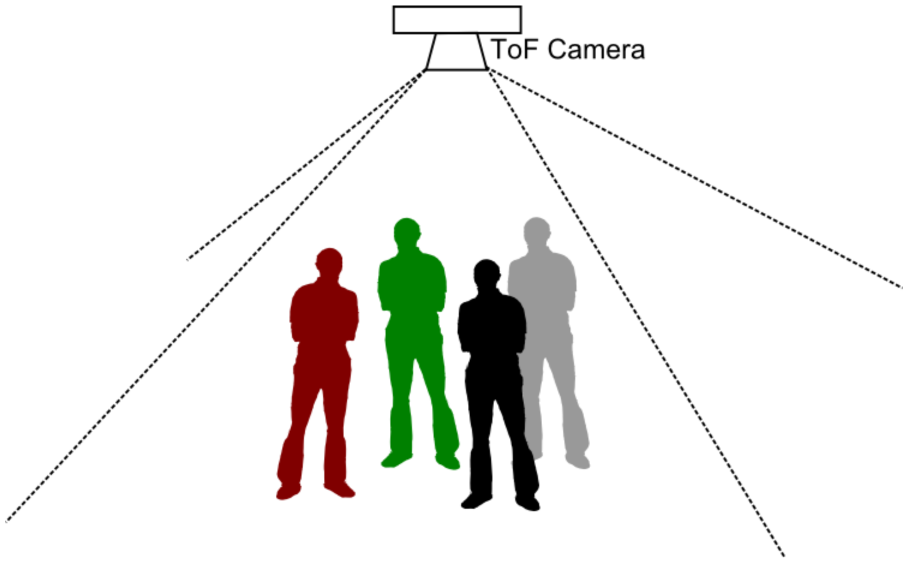


Figure 15. People Counting and Identification

8.2.3.1 Design Requirements

Table 5. People Counting and Identification Requirements

SPECIFICATION	VALUE	UNITS	COMMENTS
Depth resolution	1.5	Percentage of distance	To obtain skeletal structure and gait accurately and identify humans from other objects.
Frame rate	15	Frame per second	Reasonable update rate for moderate object movement speeds
Field of view	100.0 x 83.6	Degrees (H X V)	Higher FoVs are better for more coverage but worse from a power requirement point of view
Minimum distance	1	Meters	Example only, requirements may vary
Maximum distance	6	Meters	Example only, requirements may vary
Typical reflectivity of objects	40	Percentage	Assuming objects reflect very little infrared light and assuming Lambertian reflection
No of pixels	320 x 240	Rows x columns	Using full array
Ambient light	0	W × nm × m^2 around 850 nm	Indoor lighting conditions
Illumination source	Laser	—	Laser + diffuser for diffusing light uniformly through the scene

8.2.3.2 Detailed Design Procedure

Using the TI ToF estimator tool, the ToF camera design requirements can be input and the power numbers required for achieving the desired specifications can be obtained. The choice of inputs to the estimator tool is explained in the following section.

8.2.3.2.1 Frequencies of Operation

The frequencies of operation are limited by the sensor bandwidth because the illumination source is a laser. Frequencies around 75 MHz can be used to obtain a good demodulation figure of merit. Two frequencies are used to implement de-aliasing and extend the unambiguous range because frequencies around 75 MHz provide a very short unambiguous range. The two frequencies chosen for de-aliasing are 70 MHz and 80 MHz. The unambiguous range is now given by Equation 5.

$$\text{Unambiguous Range} = \frac{C}{2 \times \text{GCD}\left(f_1, f_2\right)} = \frac{299792458.0\ \text{ms}}{2 \times \text{GCD}\left(70\ \text{MHz}, 80\ \text{MHz}\right)} = 14.990\ \text{m} \tag{5}$$

For the purpose of power requirement calculations, the average frequency of 75 MHz can be used in the estimator tool.

8.2.3.2.2 Number of Sub-Frames and Quads

In this example, one sub-frame and six quads are used to minimize the effects of the sensor reset noise. A depth resolution of 1% instead of the requirement of 1.5% is used as the resolution input to the estimator tool to allow for margins resulting from the additional noise when using de-aliasing.

8.2.3.2.3 Field of View (FoV)

Field of view in the horizontal direction is 74.4 degrees. The diagonal FoV can be calculated using Equation 6.

$$\text{FoV}\left(\text{Diagonal}\right) = 2 \times \tan^{-1}\left[\frac{5}{4} \times \tan\left(\frac{100.0}{2}\right)\right] \approx 112.3° \tag{6}$$

The ratio of 5/4 is used to represent the ratio of the diagonal length to the horizontal length of the sensor.

8.2.3.2.4 Lens

A lens with a 1/3” image circle must be chosen. The FoV of the lens must match the requirements (that is, the FoV must be equal to 112.3 degrees, as calculated in Equation 6). A lower f.no is always better. For this example, use an f.no of 1.2.

8.2.3.2.5 Integration Duty Cycle

An integration duty cycle of 70% is chosen to keep the peak illumination power requirements low. Higher peak illumination power results in a higher number of illumination elements and, thus, an increase in system cost.

8.2.3.2.6 Design Summary

A screen shot of the system estimator tool is shown in Figure 16.

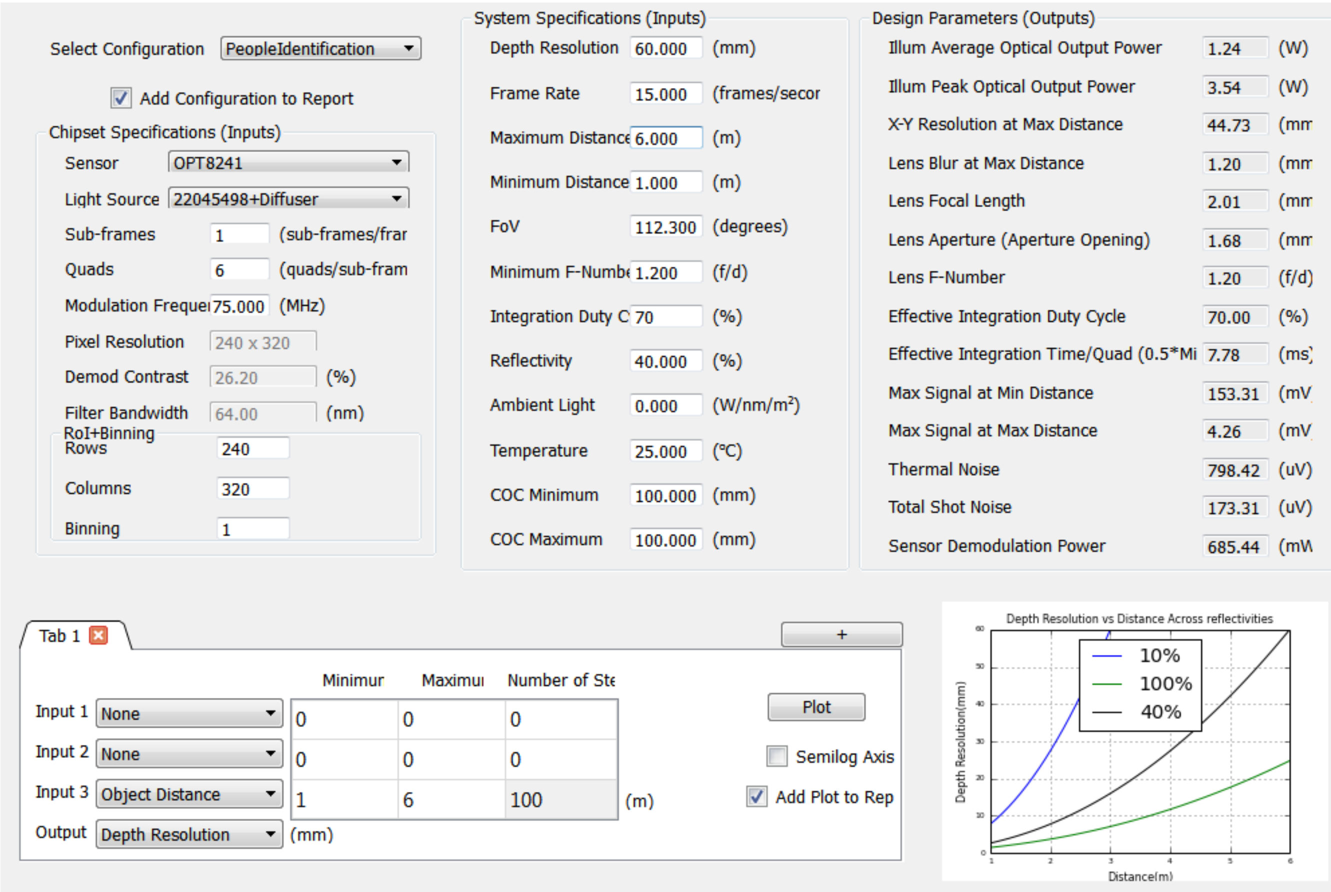
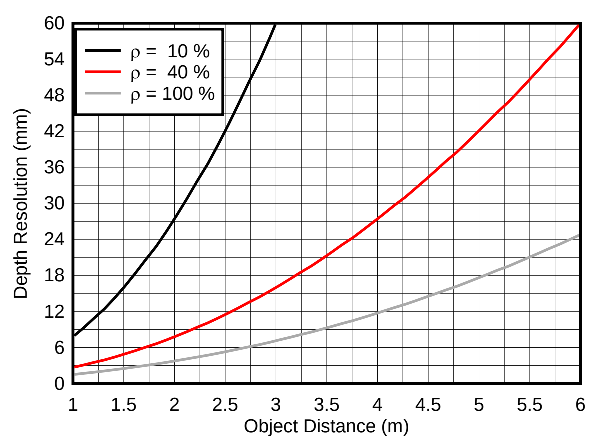


Figure 16. Screen Shot of the Estimator Tool

The illumination peak optical power of 3.54 W can be supplied using two high-power lasers.

8.2.3.3 Application Curve



ρ represents object reflectivity

Figure 17. Example People Identification Object Distance vs Depth Resolution

9 Power Supply Recommendations

The sensor reset noise is sensitive to AVDDH and PVDD supplies. Therefore, linear regulators are recommended for supplying power to the AVDD and PVDD supplies. DC-DC regulators can be used to supply power to the rest of the supplies. Ripple voltage on the VMIX and the SUB_BIAS supplies must be kept at a minimum (< 50 mV) to minimize phase noise resulting from differences between quads. The VMIX regulator must have the bandwidth to supply surge current requirements within a short time of less than 10 µs after the integration period begins because VMIX currents have a pulsed profile.

There is no strict order for the power-on or -off sequence. The VMIX supplies are recommended to be turned on after all supplies have ramped to 90% of their respective values to avoid any power-up surges resulting from high VMIX currents in a non-reset device state.

10 Layout

10.1 Layout Guidelines

10.1.1 MIX Supply Decapacitors

The VMIXH supply has a peak load current requirement of approximately 600 mA during the integration phase. Moreover, a break-before-make circuit is used during the reversal of the demodulation polarity to avoid high through currents. The break-before-make strategy results in a pulse with a drop and a subsequent rise of demodulation current. The pulse duration is typically approximately 1 ns. In order to effectively support the rise in currents, VMIXH decoupling capacitors must be placed very close to the package. Furthermore, use multiple capacitors to reduce the effect of equivalent series inductance and resistance of the decoupling capacitors. Use a combination of 10-nF and 1-nF capacitors per VMIXH pin. Using vias for routing the trace from decoupling capacitors to the package pins must be avoided.

10.1.2 LVDS Transmitters

Each LVDS data output pair must be routed as a 100-Ω differential pair. When used with the OPT9221, 100-Ω termination resistors must be placed close to the OPT9221.

10.1.3 Optical Centering

The lens mount placement on the printed circuit board (PCB) must be such that the lens optical center aligns with the pixel array optical center. Note that the pixel array center is different from the package center.

Layout Guidelines (continued)

10.1.4 Image Orientation

The sensor orientation for obtaining an upright image is shown in Figure 18.

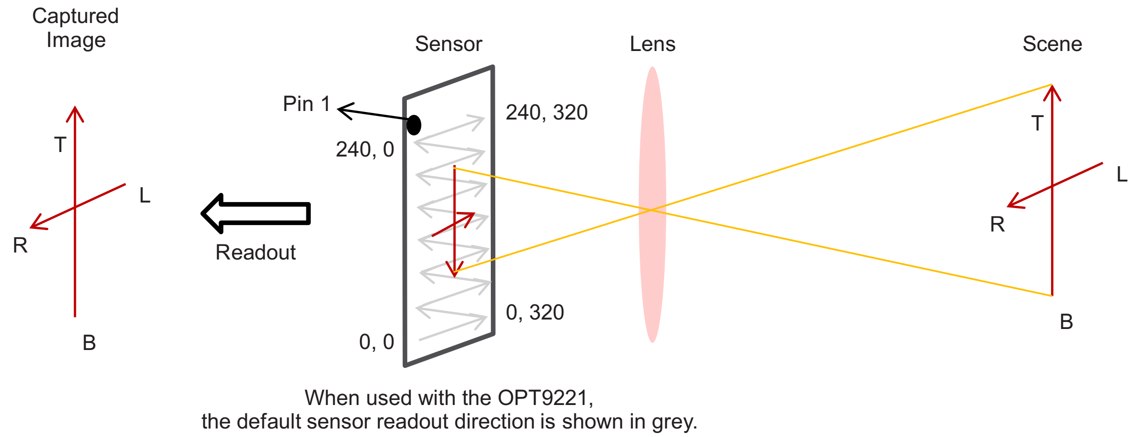


Figure 18. Sensor Orientation for Obtaining an Upright Image

10.1.5 Thermal Considerations

In some applications, special care must be taken to avoid high sensor temperatures because demodulation power is considerably high for the size of the package. Lower sensor temperatures help lower the thermal noise floor as well as reduce the leakage currents. Two recommended methods for achieving better package to PCB thermal coupling are listed below:

- Use a thermal pad below the sensor on both sides of the PCB with stitched vias.
- Use a compatible underfill.

10.2 Layout Example

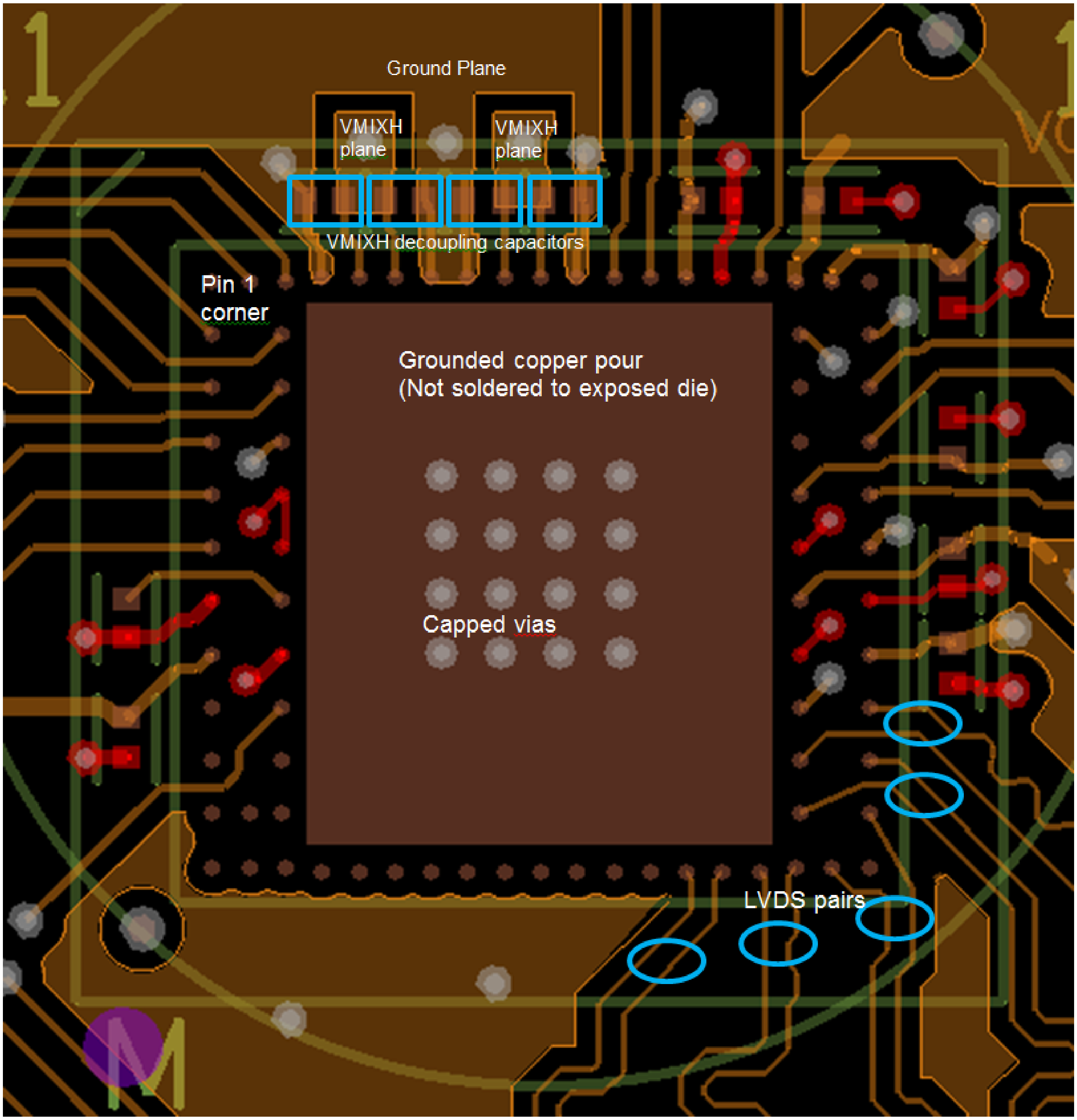


Figure 19. Example Layout

10.3 Mechanical Assembly Guidelines

10.3.1 Board-Level Reliability

TI chip-on-glass products are designed and tested with underfill to ensure excellent board-level reliability in intended applications. If a customer chooses to underfill a chip-on-glass product, following the guidelines below is recommended to maximize the board level reliability:

- The underfill material must extend partially up the package edges. Underfill that ends at the bottom (ball side) of the die degrades reliability.
- The underfill material must have a coefficient of thermal expansion (CTE) closely matched to the CTE of the solder interconnect.
- The underfill material must have a glass transition temperature (Tg) above the expected maximum exposure temperature.

Thermoset ME-525 is a good example of a compatible underfill.

10.3.2 Handling

To avoid dust particles on the sensor, the sensor tray must only be opened in a cleanroom facility. In case of accidental exposure to dust, the recommended method to clean the sensors is to use an IPA solution with a micro-fiber cloth swab with no lint. Do not handle the sensor edges with hard or abrasive materials (such as metal tweezers) because the sensor package has a glass outline. Such handling may lead to cracks that can negatively affect package reliability and image quality.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

OPT9221 Data Sheet, SBAS703

Introduction to the Time-of-Flight (ToF) System Design, SBAU219

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPT8241NBN	ACTIVE	COG	NBN	78	240	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	OPT8241	Samples
OPT8241NBNL	ACTIVE	COG	NBN	78	2400	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	OPT8241	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

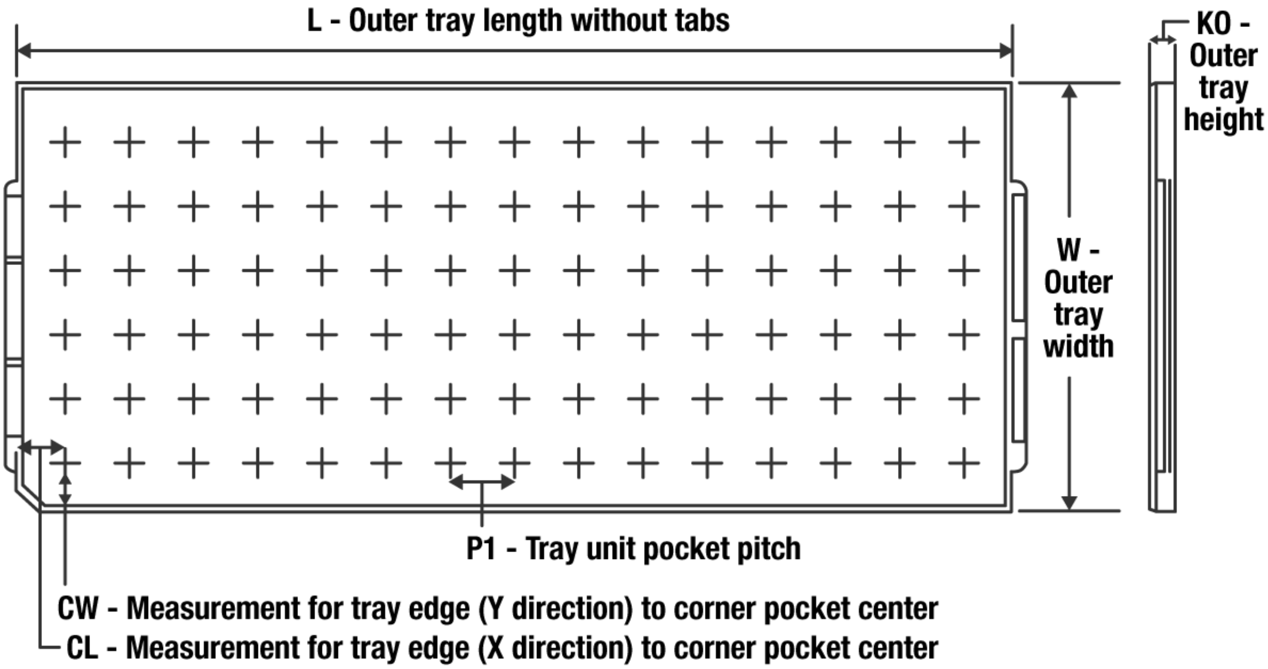
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

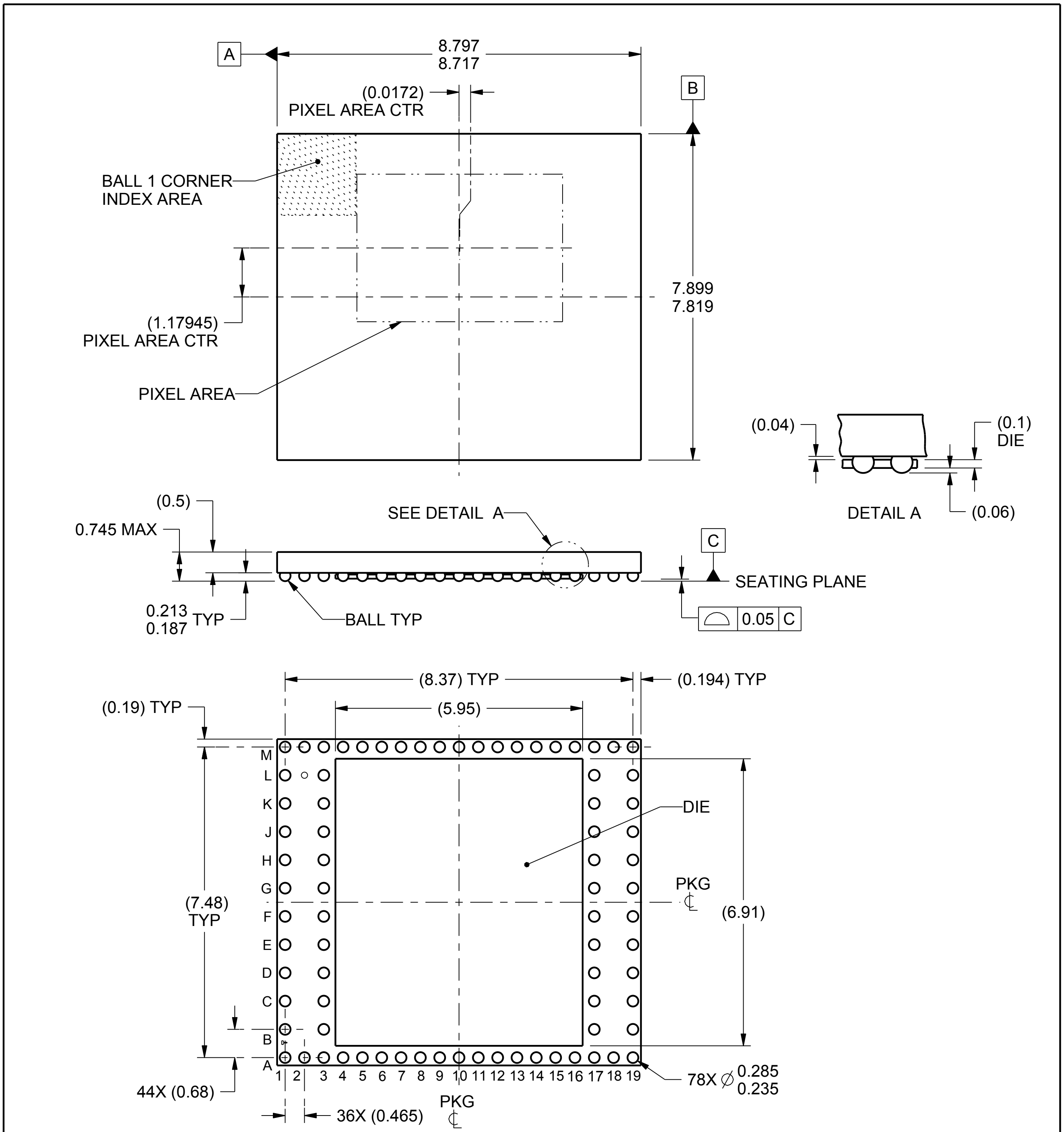
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

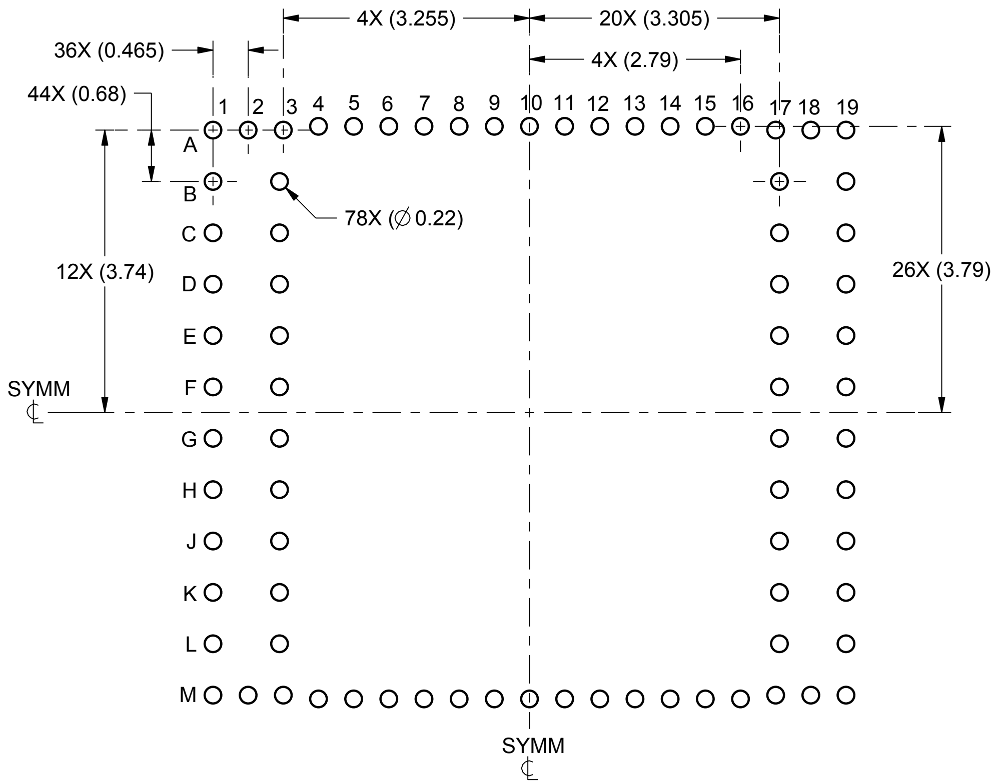
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
OPT8241NBN	NBN	COG	78	240	10 x 24	150	315	135.9	7620	12.75	10.58	13.75
OPT8241NBNL	NBN	COG	78	2400	10 x 24	150	315	135.9	7620	12.75	10.58	13.75



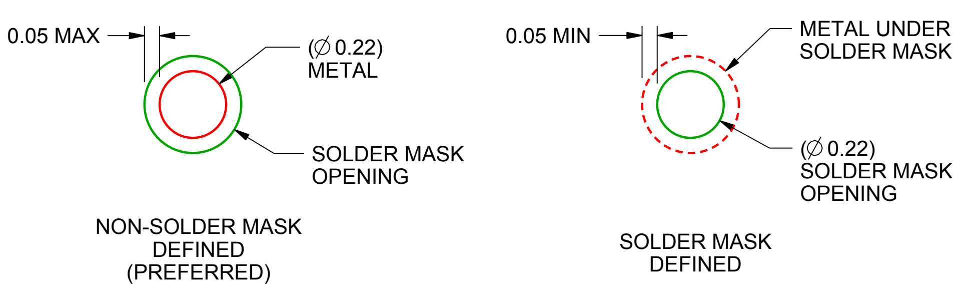
4222085/A 06/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.



LAND PATTERN EXAMPLE
SCALE:10X

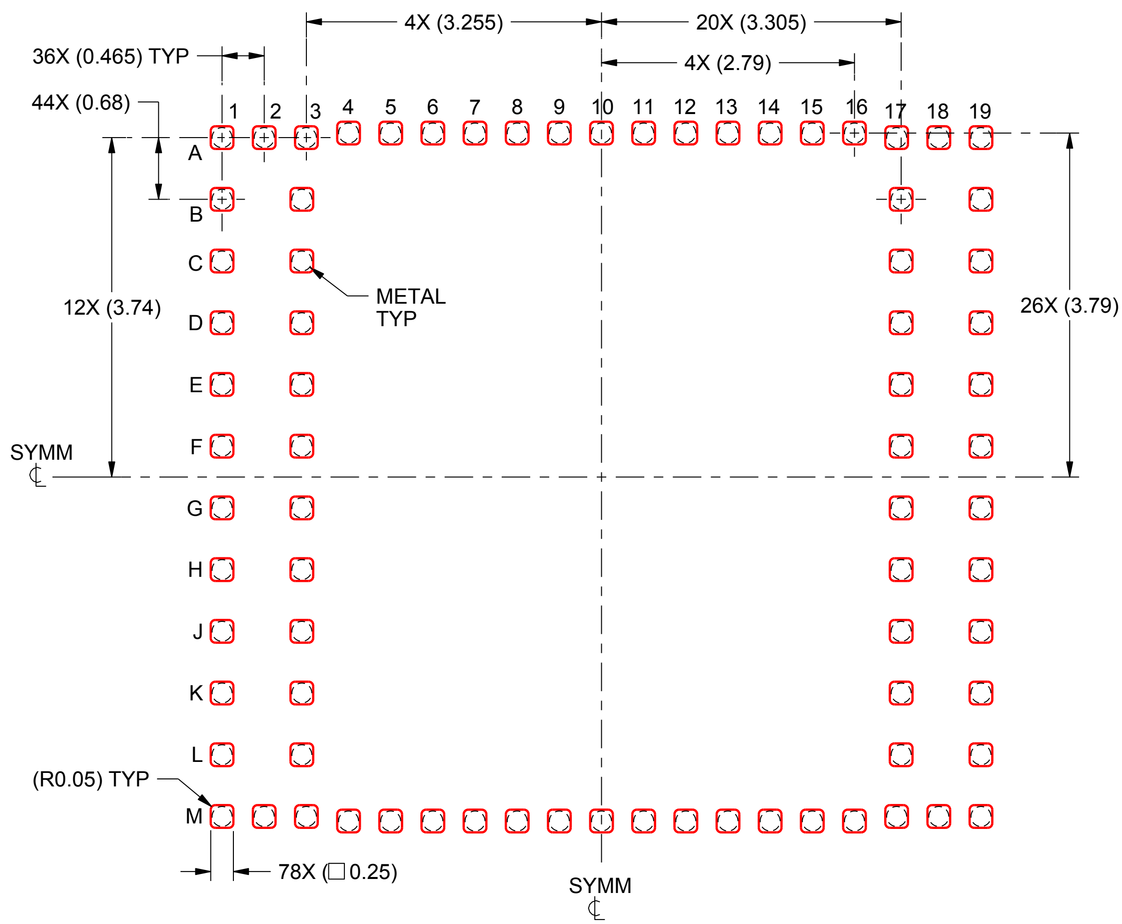


SOLDER MASK DETAILS
NOT TO SCALE

4222085/A 06/2015

NOTES: (continued)

5. PCB pads shift from original positions to prevent solder balls from touching sensor. X and Y direction: 0.05 mm. Corner pads: 0.03 mm.
6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SSYZ015 (www.ti.com/lit/ssyz015).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:12X

4222085/A 06/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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