

## Features

- 8-bit Multiplexed Addresses/Outputs
- Fast Read Access Time – 70 ns
- Dual Voltage Range Operation
  - Low-voltage Power Supply Range, 3.0V to 3.6V, or
  - Standard 5V  $\pm$  10% Supply Range
- Pin Compatible with Standard AT27C520
- Low-power CMOS Operation
  - 20  $\mu$ A Max Standby for ALE =  $V_{IH}$  and  $V_{CC}$  = 3.6V
  - 29 mW Max Active at 5 MHz for  $V_{CC}$  = 3.6V
- JEDEC Standard Packages
  - 20-lead TSSOP
  - 20-lead SOIC
- High-reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latch-up Immunity
- Rapid Programming Algorithm – 50  $\mu$ s/Byte (Typical)
- CMOS- and TTL-compatible Inputs and Outputs
  - JEDEC Standard for LVTTTL
- Integrated Product Identification Code
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

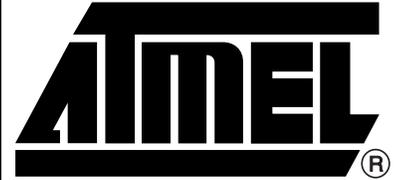
## 1. Description

The AT27LV520 is a low-power, high-performance, 524,288-bit one-time programmable read-only memory (OTP EPROM) organized 64K by eight bits. It incorporates latches for the eight lower order address bits to multiplex with the eight data bits. This minimizes system chip count, reduces cost, and simplifies the design of multiplexed bus systems. It requires only one power supply in the range of 3.0V to 3.6V for normal read mode operation, making it ideal for fast, portable systems using battery power. Any byte can be accessed in less than 70 ns.

The AT27LV520 is available in 20-lead TSSOP and 20-lead SOIC, one-time programmable (OTP) plastic packages.

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3.3V supply. At  $V_{CC}$  = 3.0V, any byte can be accessed in less than 70 ns. With a typical power dissipation of only 18 mW at 5 MHz and  $V_{CC}$  = 3.3V, the AT27LV520 consumes less than one fifth the power of a standard 5V EPROM. Standby mode is achieved by asserting ALE high. Standby mode supply current is typically less than 1  $\mu$ A at 3.3V.

The AT27LV520 operating with  $V_{CC}$  at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at  $V_{CC}$  = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.



**512K (64K x 8)  
Multiplexed  
Addresses/  
Outputs  
Low-voltage  
OTP EPROM**

**AT27LV520**



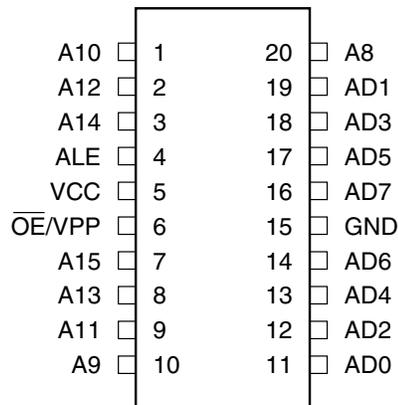


Atmel's AT27LV520 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50  $\mu$ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages. The AT27LV520 programs exactly the same way as a standard 5V AT27C520 and uses the same programming equipment.

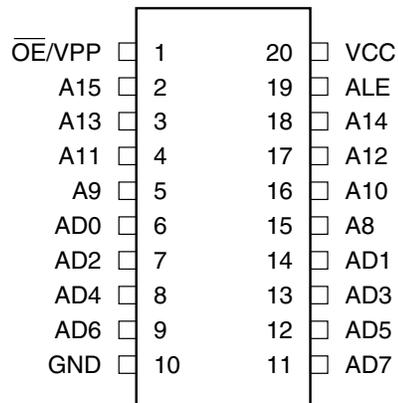
## 2. Pin Configurations

Pin Name	Function
A8 - A15	Addresses
AD0 - AD7	Addresses/Outputs
$\overline{OE}$ /VPP	Output Enable/Program Supply
ALE	Address Latch Enable

### 2.1 20-lead TSSOP Top View



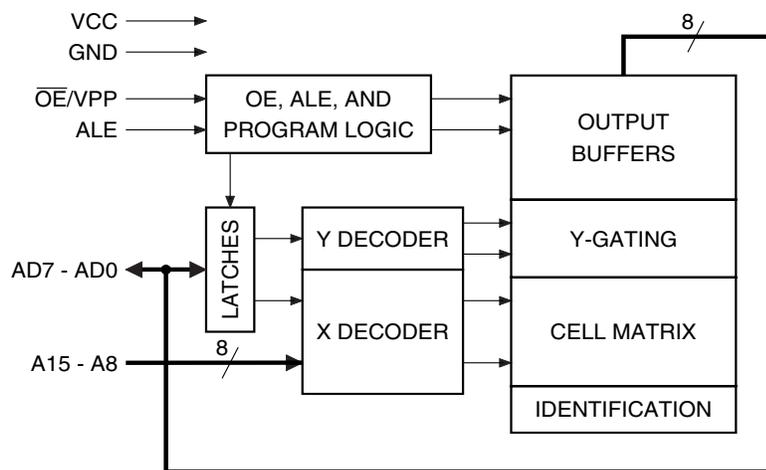
### 2.2 20-lead SOIC Top View



### 3. System Considerations

Switching under active conditions may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu\text{F}$  high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu\text{F}$  bulk electrolytic capacitor should be utilized, again connected between the  $V_{CC}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

### 4. Block Diagram



### 5. Absolute Maximum Ratings\*

Temperature under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
$V_{PP}$ Supply Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75\text{V}$  DC which may overshoot to +7.0V for pulses of less than 20 ns.



## 6. Operating Modes

Mode/Pin	ALE	$\overline{OE}/V_{PP}$	A8 - A15	AD0 - AD7
Read <sup>(2)</sup>	$V_{IL}$	$V_{IL}$	Ai	$D_{OUT}$
Output Disable <sup>(2)</sup>	$V_{IL}/V_{IH}$	$V_{IH}$	X <sup>(1)</sup>	High Z/A0 - A7
Standby	$V_{IH}$	$V_{IH}$	Ai	A0 - A7
Address Latch Enable <sup>(2)</sup>	$V_{IH}$	$V_{IH}$	X	A0 - A7
Rapid Program <sup>(3)</sup>	$V_{IH}$	$V_{PP}$	Ai	$D_{IN}$
Product Identification <sup>(4)</sup>	$V_{IL}$	$V_{IL}$	A9 = $V_H$ <sup>(5)</sup> A8 = $V_{IH}$ or $V_{IL}$ A10 - A15 = $V_{IL}$	Identification Code

- Notes:
- X can be  $V_{IL}$  or  $V_{IH}$ .
  - Read, output disable, and standby modes require  $3.0V \leq V_{CC} \leq 3.6V$ , or  $4.5V \leq V_{CC} \leq 5.5V$ .
  - Refer to Programming Characteristics.
  - $V_H = 12.0 \pm 0.5V$ .
  - Two identifier bytes may be selected. All A8 - A15 inputs are held low ( $V_{IL}$ ), except A9 which is set to  $V_H$  and A8 which is toggled low ( $V_{IL}$ ) to select the Manufacturer's Identification byte and high ( $V_{IH}$ ) to select the Device Code byte.

## 7. DC and AC Operating Conditions for Read Operation

	AT27LV520-70	AT27LV520-90
Industrial Operating Temp. (Case)	-40°C - +85°C	-40°C - +85°C
$V_{CC}$ Supply	3.0V to 3.6V	3.0V to 3.6V
	5V $\pm$ 10%	5V $\pm$ 10%

## 8. DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
<b><math>V_{CC} = 3.0V</math> to <math>3.6V</math></b>					
$I_{LI}$	Input Load Current	$V_{IN} = 0V$ to $V_{CC}$		$\pm 1$	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0V$ to $V_{CC}$		$\pm 5$	$\mu A$
$I_{SB}^{(1)}$	$V_{CC}$ Standby Current	ALE = $V_{CC} \pm 0.3V$ ; Ai, ADi = GND/ $V_{CC} \pm 0.3V$		20	$\mu A$
$I_{CC}$	$V_{CC}$ Active Current	f = 5 MHz, $I_{OUT} = 0$ mA, ALE = $V_{IL}$		8	mA
$V_{IL}$	Input Low Voltage		-0.6	0.8	V
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 0.5$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.0$ mA		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -2.0$ mA	2.4		V
<b><math>V_{CC} = 4.5V</math> to <math>5.5V</math></b>					
$I_{LI}$	Input Load Current	$V_{IN} = 0V$ to $V_{CC}$		$\pm 1$	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0V$ to $V_{CC}$		$\pm 5$	$\mu A$
$I_{SB}^{(1)}$	$V_{CC}$ Standby Current	ALE = $V_{CC} \pm 0.3V$ ; Ai, ADi = GND/ $V_{CC} \pm 0.3V$		100	$\mu A$
$I_{CC}$	$V_{CC}$ Active Current	f = 5 MHz, $I_{OUT} = 0$ mA, ALE = $V_{IL}$		20	mA
$V_{IL}$	Input Low Voltage		-0.6	0.8	V
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 0.5$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1$ mA		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400$ $\mu A$	2.4		V

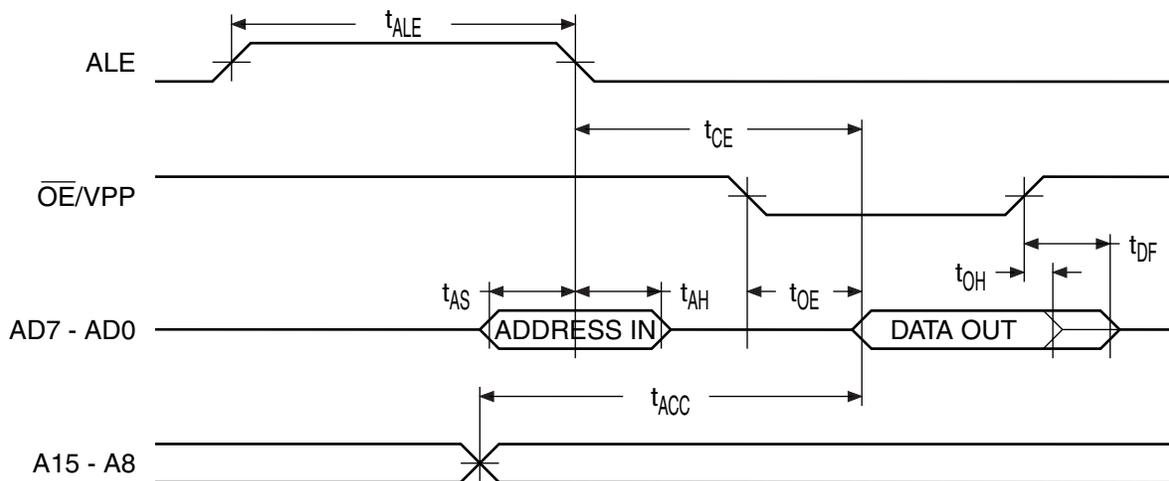
- Note: 1.  $V_{CC}$  standby current will be slightly higher with ALE, Ai, and ADi at TTL levels.

## 9. AC Characteristics for Read Operation

$V_{CC} = 3.0V$  to  $3.6V$  and  $4.5V$  to  $5.5V$

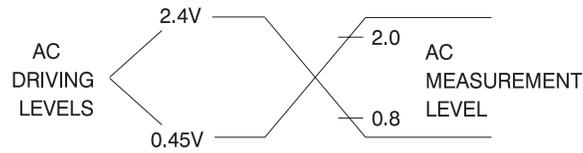
Symbol	Parameter	Condition	AT27LV520-70		AT27LV520-90		Units
			Min	Max	Min	Max	
$t_{ACC}^{(3)}$	Address to Output Delay	$ALE = \overline{OE}/V_{PP} = V_{IL}$		70		90	ns
$t_{CE}$	Address Latch Enable Low to Output Delay	Address Valid		55		70	ns
$t_{AS}$	Address Setup Time	$\overline{OE}/V_{PP} = V_{IH}$	12		15		ns
$t_{AH}$	Address Hold Time	$\overline{OE}/V_{PP} = V_{IH}$	12		15		ns
$t_{ALE}$	Address Latch Enable Width	$\overline{OE}/V_{PP} = V_{IH}$	40		45		ns
$t_{OE}^{(3)}$	$\overline{OE}/V_{PP}$ to Output Delay	$ALE = V_{IL}$		30		35	ns
$t_{DF}^{(4)(5)}$	$\overline{OE}/V_{PP}$ High to Output Float	$ALE = V_{IL}$		25		25	ns
$t_{OH}$	Output Hold from Address or $\overline{OE}/V_{PP}$ Whichever Occurred First	$ALE = V_{IL}$	7		0		ns

## 10. AC Waveforms for Read Operation<sup>(1)</sup>



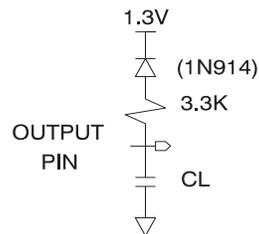
- Notes:
1. Timing measurement reference levels for all speed grades are  $V_{OL} = 0.8V$  and  $V_{OH} = 2.0V$ . Input AC drive levels are  $V_{IL} = 0.45V$  and  $V_{IH} = 2.4V$ .
  2.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{CE} - t_{OE}$  after the address is valid without impact on  $t_{CE}$ .
  3.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
  4. This parameter is only sampled and is not 100% tested.
  5. Output float is defined as the point when data is no longer driven.

## 11. Input Test Waveforms and Measurement Levels



$t_R, t_F < 20 \text{ ns (10\% to 90\%)}$

## 12. Output Test Load



Note:  $C_L = 100 \text{ pF}$  including jig capacitance.

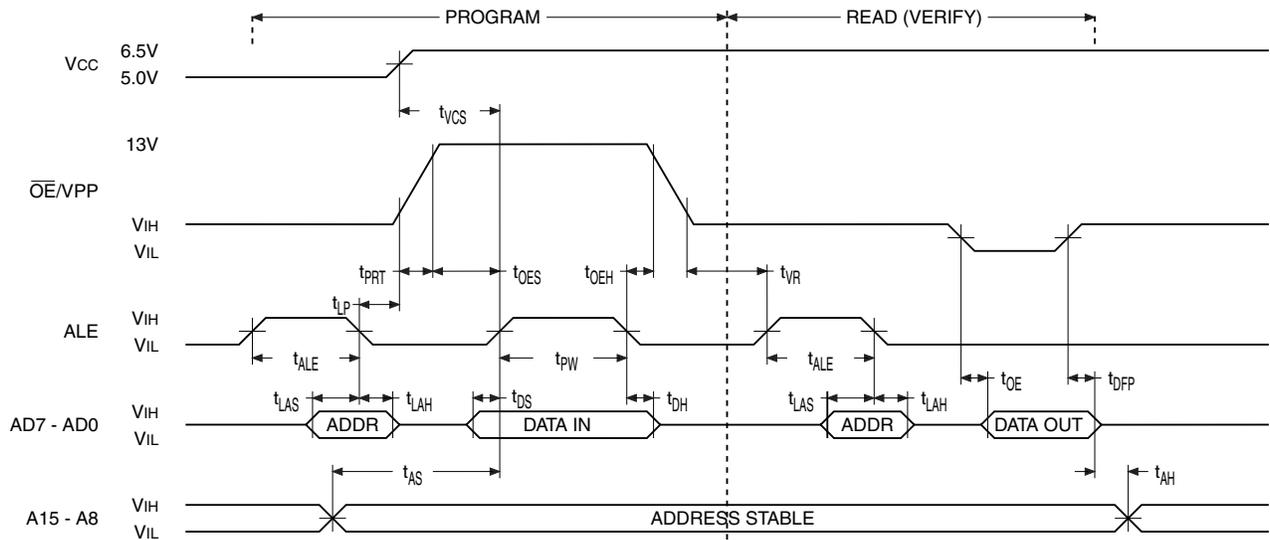
## 13. Pin Capacitance

$f = 1 \text{ MHz}, T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

### 14. Programming Waveforms



- Notes:
1. The Input Timing Reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
  2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.

### 15. DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $\overline{OE}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$I_{LI}$	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		$\pm 10$	$\mu\text{A}$
$V_{IL}$	Input Low Level		-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	$V_{CC} + 1.0$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400 \mu\text{A}$	2.4		V
$I_{CC2}$	$V_{CC}$ Supply Current (Program and Verify)			25	mA
$I_{PP2}$	$\overline{OE}/V_{PP}$ Current	$\text{ALE} = V_{IH}$		25	mA

## 16. AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $\overline{\text{OE}}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter <sup>(1)</sup>	Test Conditions	Limits		Units
			Min	Max	
$t_{ALE}$	Address Latch Enable Width	Input Rise and Fall Times: (10% to 90%) 20 ns  Input Pulse Levels: 0.45V to 2.4V  Input Timing Reference Level: 0.8V to 2.0V  Output Timing Reference Level: 0.8V to 2.0V	500		ns
$t_{LAS}$	Latched Address Setup Time		100		ns
$t_{LAH}$	Latched Address Hold Time		100		ns
$t_{LP}$	ALE Low to $\overline{\text{OE}}/V_{PP}$ High Voltage Delay		2		$\mu\text{s}$
$t_{OES}$	$\overline{\text{OE}}/V_{PP}$ Setup Time		2		$\mu\text{s}$
$t_{OEH}$	$\overline{\text{OE}}/V_{PP}$ Hold Time		2		$\mu\text{s}$
$t_{DS}$	Data Setup Time		2		$\mu\text{s}$
$t_{DH}$	Data Hold Time		2		$\mu\text{s}$
$t_{PW}$	ALE Program Pulse Width <sup>(2)</sup>		47.5	52.5	$\mu\text{s}$
$t_{VR}$	$\overline{\text{OE}}/V_{PP}$ Recovery Time		2		$\mu\text{s}$
$t_{VCS}$	$V_{CC}$ Setup Time		2		$\mu\text{s}$
$t_{OE}$	Data Valid from $\overline{\text{OE}}/V_{PP}$			150	ns
$t_{DFP}$	$\overline{\text{OE}}/V_{PP}$ High to Output Float Delay <sup>(3)</sup>		0	130	ns
$t_{AS}$	Address Setup Time		2		$\mu\text{s}$
$t_{AH}$	Address Hold Time		0		$\mu\text{s}$
$t_{PRT}$	$\overline{\text{OE}}/V_{PP}$ Pulse Rise Time During Programming	50		ns	

- Notes:
- $V_{CC}$  must be applied simultaneously or before  $\overline{\text{OE}}/V_{PP}$  and removed simultaneously or after  $\overline{\text{OE}}/V_{PP}$ .
  - Program Pulse width tolerance is  $50 \mu\text{sec} \pm 5\%$ .
  - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.

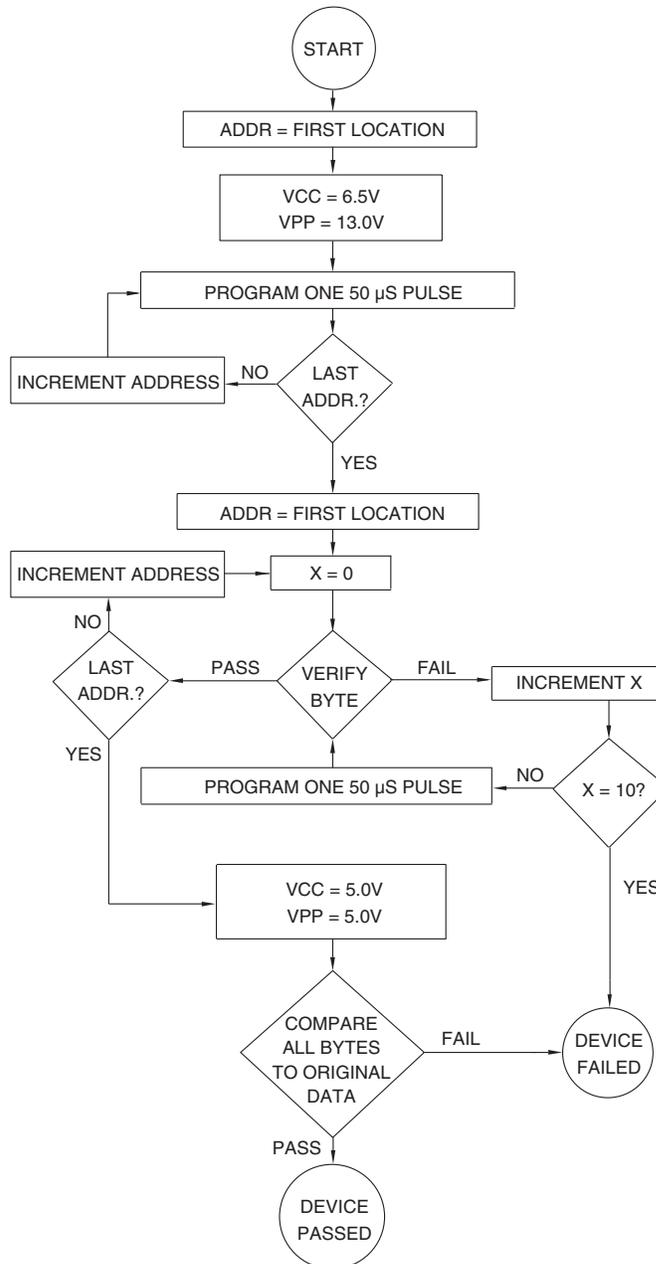
## 17. Atmel's AT27LV520 Integrated Product Identification Code

Codes	Pins									Hex Data
	A8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	1	1	1	0	1	9D

- Note: 1. The AT27LV520 has the same product identification code as the AT27C520. Both are programming compatible.

## 18. Rapid Programming Algorithm

A 50  $\mu$ s ALE pulse width is used to program. The address is set to the first location.  $V_{CC}$  is raised to 6.5V and  $\overline{OE}/V_{PP}$  is raised to 13.0V. Each address is first programmed with one 50  $\mu$ s ALE pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50  $\mu$ s pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $\overline{OE}/V_{PP}$  is then lowered to  $V_{IH}$  and  $V_{CC}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.





## 19. Ordering Information

### 19.1 Standard Package

$t_{ACC}$ (ns)	$I_{CC}$ (mA) Active	Ordering Code	Package	Operation Range
70	8	AT27LV520-70SI	20S	Industrial (-40°C to +85°C)
		AT27LV520-70XI	20X	
90	8	AT27LV520-90SI	20S	Industrial (-40°C to +85°C)
		AT27LV520-90XI	20X	

### 19.2 Green Package (Pb/Halide-free)

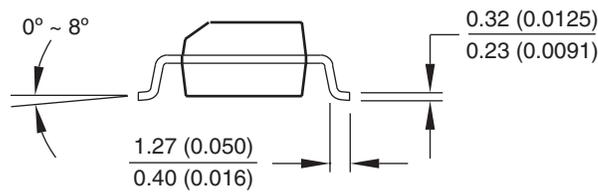
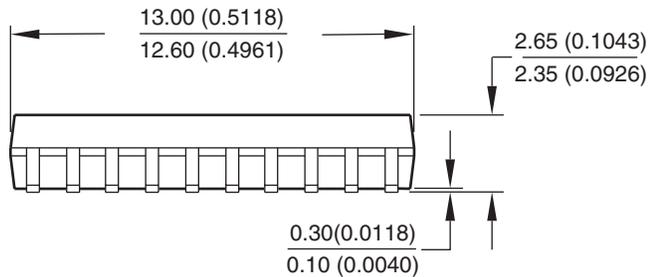
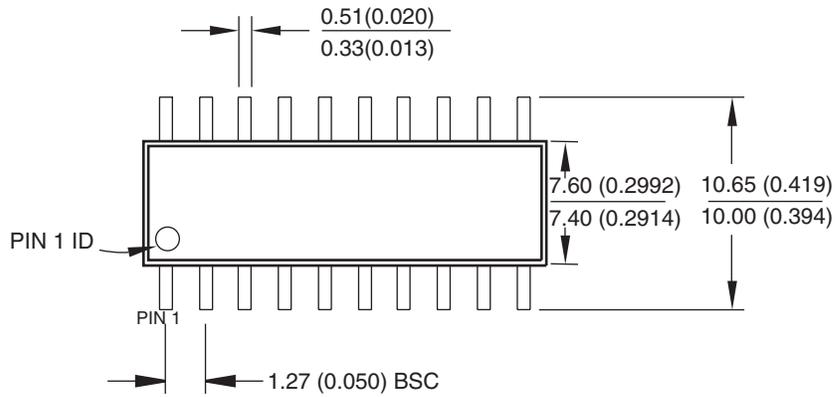
$t_{ACC}$ (ns)	$I_{CC}$ (mA) Active	Ordering Code	Package	Operation Range
70	8	AT27LV520-70SU	20S	Industrial (-40°C to +85°C)
		AT27LV520-70XU	20X	
90	8	AT27LV520-90XU	20X	Industrial (-40°C to +85°C)

Package Type	
<b>20S</b>	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
<b>20X</b>	20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline (TSSOP)

20. Packaging Information

20.1 20S – SOIC

Dimensions in Millimeters and (Inches).  
 Controlling dimension: Inches.  
 JEDEC Standard MS-013



10/23/03

**AMEL** 2325 Orchard Parkway  
 San Jose, CA 95131

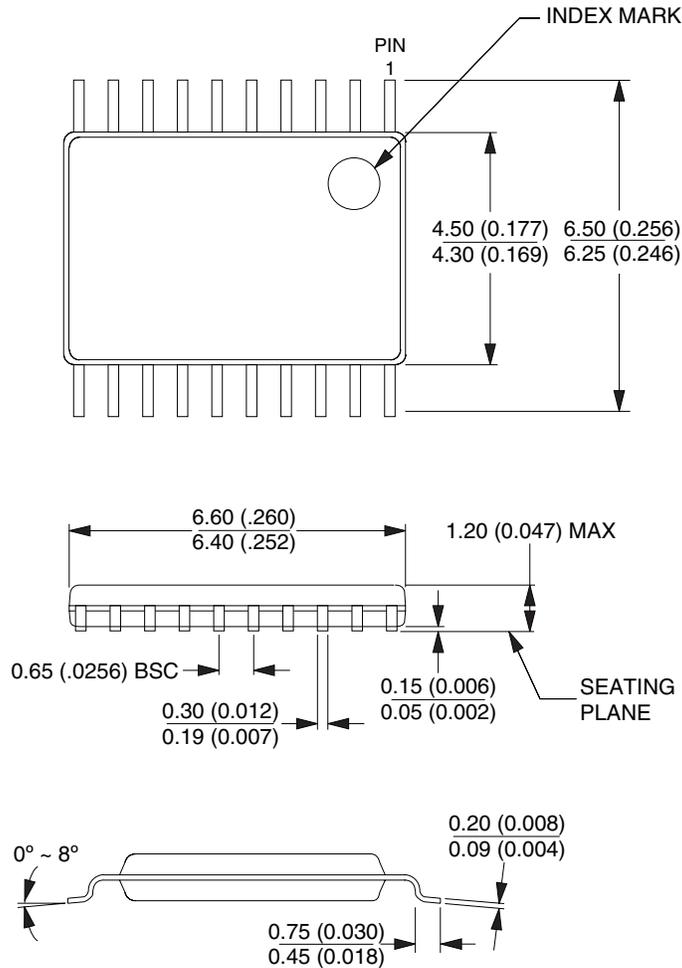
**TITLE**  
**20S, 20-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC)**

**DRAWING NO.**  
 20S

**REV.**  
 B

## 20.2 20X – TSSOP

Dimensions in Millimeters and (Inches).  
 Controlling dimension: Millimeters.  
 JEDEC Standard MO-153 AC



10/23/03



2325 Orchard Parkway  
 San Jose, CA 95131

**TITLE**

**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width,  
 Plastic Thin Shrink Small Outline Package (TSSOP)

**DRAWING NO.**

20X

**REV.**

C



## Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## Regional Headquarters

### Europe

Atmel Sarl  
Route des Arsenalux 41  
Case Postale 80  
CH-1705 Fribourg  
Switzerland  
Tel: (41) 26-426-5555  
Fax: (41) 26-426-5500

### Asia

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

### Japan

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Atmel Operations

### Memory

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

### Microcontrollers

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

La Chantrerie  
BP 70602  
44306 Nantes Cedex 3, France  
Tel: (33) 2-40-18-18-18  
Fax: (33) 2-40-18-19-60

### ASIC/ASSP/Smart Cards

Zone Industrielle  
13106 Rousset Cedex, France  
Tel: (33) 4-42-53-60-00  
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park  
Maxwell Building  
East Kilbride G75 0QR, Scotland  
Tel: (44) 1355-803-000  
Fax: (44) 1355-242-743

### RF/Automotive

Theresienstrasse 2  
Postfach 3535  
74025 Heilbronn, Germany  
Tel: (49) 71-31-67-0  
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

### Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine  
BP 123  
38521 Saint-Egreve Cedex, France  
Tel: (33) 4-76-58-30-00  
Fax: (33) 4-76-58-34-80

---

## Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

**Disclaimer:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© Atmel Corporation 2005. All rights reserved. Atmel®, logo and combinations thereof, Everywhere You Are® and others, are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.



Printed on recycled paper.

0911F-EPROM-10/05