

ITS4880R

Smart Power High-Side-Switch for Industrial Applications, Eight Channels: 8 x 200 mΩ

Industrial PROFET

Data Sheet

Rev. 1.2 2014-12-10

Standard Power

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Smart Power High-Side-Switch for Industrial Applications, Eight Channels: 8 x 200 mΩ

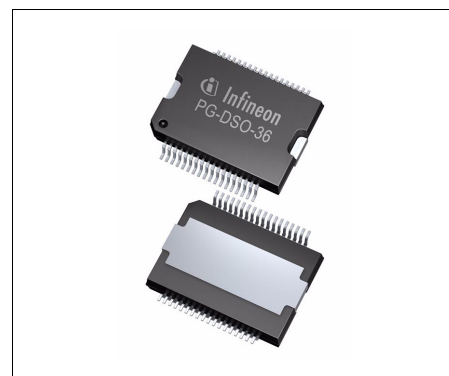
ITS4880R



1 Overview

Features

- Output current 0.625 A per channel
- Short circuit protection
- Maximum current internally limited
- Overload protection
- Input protection
- Overvoltage protection (including load dump)
- Undervoltage shutdown with auto-restart and hysteresis
- Switching inductive loads
- Thermal shutdown with restart
- Thermal independence of separate channels
- ESD-Protection
- Loss of GND and loss of V_{bb} protection
- Very low standby current
- Reverse battery protection
- Programmable input for CMOS or $V_{bb}/2$
- Common diagnostic output (current output for overtemperature)
- Green Product (RoHS Compliant)



PG-DSO-36-26

Application

- Output driver for industrial applications (PLC)
- All types of resistive, inductive and capacitive loads
- μ C or optocoupler compatible power switch for 24 V DC industrial applications
- Replaces electromechanical relays and discrete circuits

General Description

N channel vertical power FET with charge pump, ground referenced CMOS or $V_{bb}/2$ compatible input and common diagnostic feedback, monolithically integrated in Smart SIPMOS® technology. Providing embedded protective functions.

Product Summary

Overvoltage protection: $V_{bbAZmin} = 47$ V

Operating voltage: 11 V < $V_{bb(on)}$ < 45 V

On-state resistance: $R_{ON} = 200$ mΩ

Operating Temperature: $T_a = -30$ °C to 85 °C

Type	Package	Marking
ITS4880R	PG-DSO-36-26	ITS 4880R

Block Diagram

2 Block Diagram

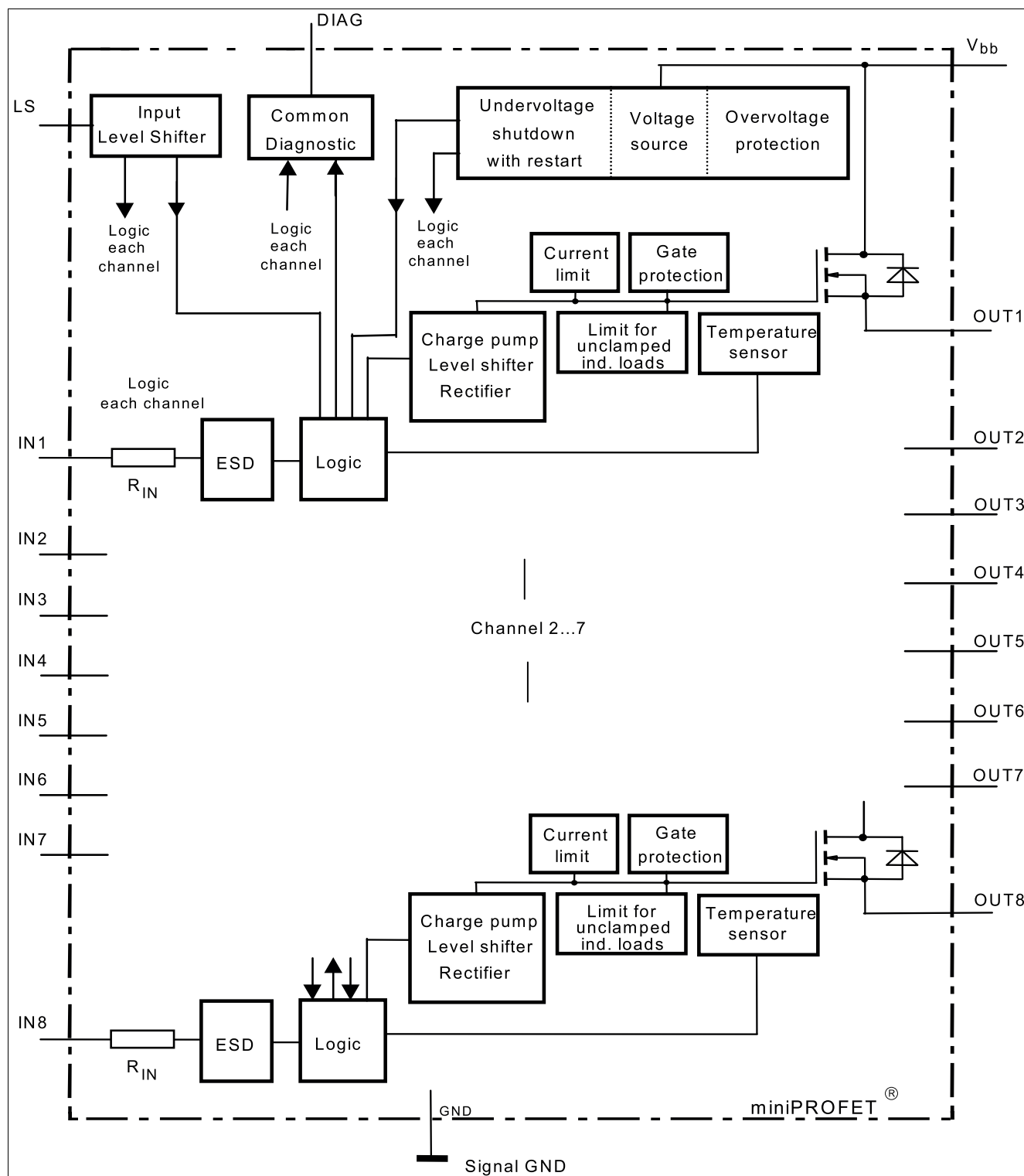


Figure 1 Block diagram

Pin Configuration

3 Pin Configuration

1,2,4,5	NC	not connected
3	LS	Enable pin for switching the input-levels to V_{bb}
6	IN1	Input, activates channel 1 in case of logic high signal
7	IN2	Input, activates channel 2 in case of logic high signal
8	IN3	Input, activates channel 3 in case of logic high signal
9	IN4	Input, activates channel 4 in case of logic high signal
10	IN5	Input, activates channel 5 in case of logic high signal
11	IN6	Input, activates channel 6 in case of logic high signal
12	IN7	Input, activates channel 7 in case of logic high signal
13	IN8	Input, activates channel 8 in case of logic high signal
14-18	NC	not connected
19	GND	Logic ground
20	DIAG	Common diagnostic output for overtemperature
21	OUT8	High-side output of channel 8
22	OUT8	High-side output of channel 8
23	OUT7	High-side output of channel 7
24	OUT7	High-side output of channel 7
25	OUT6	High-side output of channel 6
26	OUT6	High-side output of channel 6
27	OUT5	High-side output of channel 5
28	OUT5	High-side output of channel 5
29	OUT4	High-side output of channel 4
30	OUT4	High-side output of channel 4
31	OUT3	High-side output of channel 3
32	OUT3	High-side output of channel 3
33	OUT2	High-side output of channel 2
34	OUT2	High-side output of channel 2
35	OUT1	High-side output of channel 1
36	OUT1	High-side output of channel 1
TAB	V_{bb}	Positive power supply voltage

General Product Characteristics

4 General Product Characteristics

4.1 Maximum Ratings

Table 1 Maximum ratings at $T_j = -40\text{ °C}...135\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	V_{bb}	-1 ¹⁾	–	45	V	–	–
Continuous input Voltage ²⁾	V_{IN}	-10	–	V_{bb}	V	–	–
Continuous input Voltage at LS-pin	V_{LS}	-1	–	V_{bb}	V	–	–
Load current (Short circuit current see Page 9)	I_L	–	–	–	A	self limited	–
Current through input pin (DC), each channel	I_{IN}	-5	–	5	mA	–	–
Reverse current through GND-pin ¹⁾	$-I_{GND}$	–	–	1.6	A	–	–
Junction Temperature	T_j	–	–	–	°C	internal limited	–
Operating Temperature	T_a	-30	–	85	°C	–	–
Storage Temperature	T_{stg}	-40	–	105	°C	–	–
Power dissipation ³⁾	P_{tot}	–	–	3.3	W	–	–
Inductive load switch-off energy dissipation ⁴⁾ , $T_j = 125\text{ °C}$, $I_L = 0.625\text{ A}$, one channel active	E_{AS}	–	–	10	J	single pulse	–
Inductive load switch-off energy dissipation ⁴⁾ , $T_j = 125\text{ °C}$, $I_L = 0.625\text{ A}$, all channels simultaneously active	E_{AS}	–	–	1	J	single pulse	–
Load dump protection ⁴⁾ $V_{Loaddump}^{5)} = V_A + V_S$, $V_{IN} = \text{low or high}$, $t_d = 400\text{ ms}$, $R_I = 2\text{ }\Omega$, $R_L = 27\text{ }\Omega$, $V_A = 13.5\text{ V}$	$V_{Loaddump}$	–	–	90	V	–	–
Load dump protection ⁴⁾ $V_{Loaddump}^{5)} = V_A + V_S$, $V_{IN} = \text{low or high}$, $t_d = 350\text{ ms}$, $R_I = 2\text{ }\Omega$, $R_L = 47\text{ }\Omega$, $V_A = 27\text{ V}$	$V_{Loaddump}$	–	–	117	V	–	–
Electrostatic discharge voltage (Human Body Model) according to ANSI EOS/ESD - S5.1 - 1993, ESD STM5.1 - 1998; Input pin, LS pin, Common diagnostic pin	V_{ESD}	-1	–	1	kV	–	–

General Product Characteristics

Table 1 Maximum ratings at $T_j = -40\text{ °C}...135\text{ °C}$, unless otherwise specified (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Electrostatic discharge voltage (Human Body Model) according to ANSI EOS/ESD - S5.1 - 1993, ESD STM5.1 - 1998; all other pins	V_{ESD}	-5	–	5	kV	–	–
Continuous reverse drain current ^{1) 4)} , each channel	I_S	–	–	4	A	–	–

1) defined by P_{tot}

2) At $V_{\text{IN}} > V_{\text{bb}}$ the input current is not allowed to exceed $\pm 5\text{ mA}$.

3) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

4) not subject to production test, specified by design

5) V_{Loadump} is set up without the DUT connected to the generator per ISO 7637-1 and DIN 40839. Supply voltages higher than $V_{\text{bb(AZ)}}$ require an external current limit for the GND pin, e.g. with a 150 Ω resistor in GND connection. A resistor for the protection of the input is integrated.

4.2 Thermal Characteristics

Table 2 Thermal Characteristics at $T_j = -25\text{ °C}...125\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance junction to case	R_{thJC}	–	–	1.5	K/W	–	–
Thermal resistance @ min. footprint	$R_{\text{th(JA)}}$	–	–	50	K/W	–	–
Thermal resistance @ 6 cm ² cooling area ¹⁾	$R_{\text{th(JA)}}$	–	–	38	K/W	–	–

1) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics

5 Electrical Characteristics

5.1 Load Switching Capabilities and Characteristics

Table 3 Load Switching Capabilities and Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
On-state resistance	R_{ON}	–	150	200	mΩ	$T_j = 25\text{ °C}$ $I_L = 0.5\text{ A}$	–
On-state resistance	R_{ON}	–	270	320	mΩ	$T_j = 125\text{ °C}$	–
Turn-on-time to 90% V_{OUT}	t_{on}	–	50	100	μs	$R_L = 47\text{ Ω}$, $V_{IN} = 0\text{ to }10\text{ V}$	–
Turn-off-time to 10% of V_{OUT}	t_{off}	–	75	150	μs	$R_L = 47\text{ Ω}$, $V_{IN} = 10\text{ to }0\text{ V}$	–
Slew rate on, 10 to 30% V_{OUT}	dV/dt_{on}	–	1	2	V/μs	$R_L = 47\text{ Ω}$, $V_{bb} = 15\text{ V}$	–
Slew rate off, 70 to 40% V_{OUT}	$-dV/dt_{off}$	–	1	2	V/μs	$R_L = 47\text{ Ω}$, $V_{bb} = 15\text{ V}$	–

5.2 Operating Parameters

Table 4 Operating Parameters at $T_j = -25\text{ °C}...125\text{ °C}$, $V_{bb} = 15...30\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Operating Voltage	$V_{bb(on)}$	11	–	45	V	–	–
Undervoltage shutdown	$V_{bb(under)}$	7	–	10.5	V	–	–
Undervoltage restart	$V_{bb(u\text{ rst})}$	–	–	11	V	–	–
Undervoltage hysteresis	$\Delta V_{bb(under)}$	–	0.5	–	V	$\Delta V_{bb(under)} = V_{bb(u\text{ rst})} - V_{bb(under)}$	–
Standby current	$I_{bb(off)}$	–	50	150	μA	–	–
Operating current ¹⁾	I_{GND}	–	5	12	mA	–	–
Leakage output current (included in $I_{bb(off)}$)	$I_{L(off)}$	–	5	10	μA	$V_{IN} = \text{low}$, each channel	–

1) Contains all input currents.

Electrical Characteristics

5.3 Protection Functions

Table 5 Protection Functions ¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Initial peak short circuit current limit	$I_{L(SCp)}$	–	–	1.9	A	$T_j = -25\text{ °C};$ $V_{bb} = 30\text{ V};$ $t_m = 700\mu\text{s}$	–
Initial peak short circuit current limit	$I_{L(SCp)}$	–	1.4	–	A	$T_j = 25\text{ °C}$	–
Initial peak short circuit current limit	$I_{L(SCp)}$	0.7	–	–	A	$T_j = 125\text{ °C}$	–
Repetitive short circuit current limit $T_j = T_{jt}$ (see timing diagrams)	$I_{L(SCr)}$	–	1.1	–	A	–	–
Output clamp (inductive load switch off) at $V_{OUT} = V_{bb} - V_{ON(CL)}$	$V_{ON(CL)}$	47	53	60	V	–	–
Oversvoltage protection ²⁾	$V_{bb(AZ)}$	47	–	–	V	–	–
Thermal overload trip temperature ³⁾	T_{jt}	135	–	–	°C	–	–
Thermal hysteresis	ΔT_{jt}	–	10	–	K	–	–

1) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

2) see also $V_{ON(CL)}$ in circuit diagram on Page 14

3) higher operating temperature at normal function for each channel available

5.4 Input

Table 6 Input at $T_j = -25\text{ °C}...125\text{ °C}$, $V_{bb} = 15...30\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Continuous input voltage ¹⁾	V_{IN}	-10	–	V_{bb}	V	–	–
Input turn-on threshold voltage CMOS ²⁾	$V_{IN(T+)}$	–	–	2.2	V	–	–
Input turn-off threshold voltage CMOS ²⁾	$V_{IN(T-)}$	0.8	–	–	V	–	–
Input turn-on threshold voltage $V_{bb}/2$ ²⁾	$V_{IN(T+)}$	–	–	$V_{bb}/2 + 1$	V	–	–

Electrical Characteristics

Table 6 Input at $T_j = -25\text{ °C} \dots 125\text{ °C}$, $V_{bb} = 15 \dots 30\text{ V}$, unless otherwise specified (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input turn-off threshold voltage $V_{bb} / 2$ ²⁾	$V_{IN(T-)}$	$V_{bb} / 2 - 1$	–	–	V	–	–
Input threshold hysteresis	$\Delta V_{IN(T)}$	–	0.3	–	V	–	–
Off state input current CMOS (each channel)	$I_{IN(off)}$	8	–	–	μA	–	–
On state input current CMOS (each channel)	$I_{IN(on)}$	–	–	70	μA	–	–
Off state input current $V_{bb} / 2$ (each channel)	$I_{IN(off)}$	80	–	–	μA	–	–
On state input current $V_{bb} / 2$ (each channel)	$I_{IN(on)}$	–	–	260	μA	–	–
Input delay time at switch on V_{bb}	$t_{d(V_{bb}on)}$	150	340	–	μs	–	–
Input resistance (see Page 14)	R_I	2	3	4	kΩ	–	–
Internal pull down resistor at LS-pin ³⁾	R_{LS}	300	800	–	kΩ	–	–

1) At $V_{IN} > V_{bb}$ the input current is not allowed to exceed $\pm 5\text{ mA}$.

2) see page [Page 13](#)

3) LS-pin is connected to V_{bb}

5.5 Diagnostic Characteristics

Table 7 Diagnostic Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Common diagnostic output current ¹⁾ (overtemperature of any channel) $T_j = 135\text{ °C}$	I_{diag}	2	3	4	mA	–	–
Common diagnostic output leakage current	$I_{diag(high)}$	–	–	2	μA	–	–

1) see Page 14

Electrical Characteristics

5.6 Reverse Battery

Table 8 Reverse Battery at $T_j = -25\text{ }^{\circ}\text{C} \dots 125\text{ }^{\circ}\text{C}$, $V_{bb} = 15 \dots 30\text{ V}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Reverse battery voltage ¹⁾	$-V_{bb}$	–	–	1	V	$R_{GND} = 0\ \Omega$	–
Reverse battery voltage	$-V_{bb}$	–	–	45	V	$R_{GND} = 150\ \Omega$	–
Diode forward on voltage	$-V_{ON}$	–	–	1.2	V	$I_F = 1.25\text{ A}$; $V_{IN} = \text{low}$, each channel	–

1) defined by P_{tot}

Application Information

6 Application Information

6.1 Truth table for common diagnostic pin (LED-driver)

Table 9 Truth table for common diagnostic pin (LED-driver)

	Input level	Output level	Diagnostic
Normal Operation	L	L	L
Normal Operation	H	H	L
Short circuit to GND	L	L	L
Short circuit to GND	H	L	L
Undervoltage	L	L	L
Undervoltage	H	L	L
Overtemperature	L	L	L
Overtemperature	H	L	H ¹⁾

1) toggling with restart

L = no diagnostic output current

H = diagnostic output current typ. 2 mA (see [Page 10](#))

Application Information

6.2 Programmable input

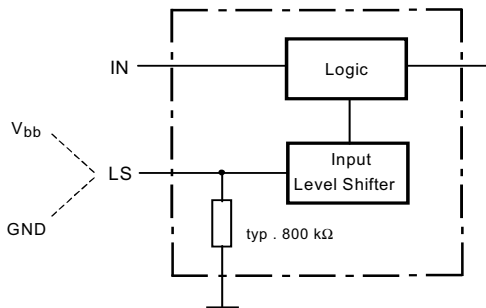


Figure 2 Programmable input

6.3 Functional description LS-Pin

With using the LS-pin it is possible to change the input turn-on and -off threshold voltage between CMOS and half supply voltage level.

Therefore you have either to connect the LS-pin to GND (state 1) or to supply voltage (state 2).

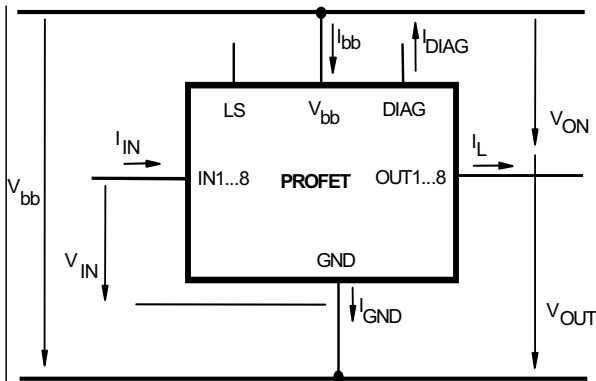
State 1: LS-Pin to GND CMOS-Input level

State 2: LS-Pin to supply voltage $V_{bb}/2$ - Input level

Application Information

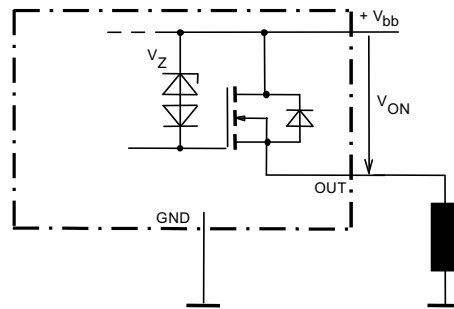
Terms

each channel



Inductive and overvoltage output clamp

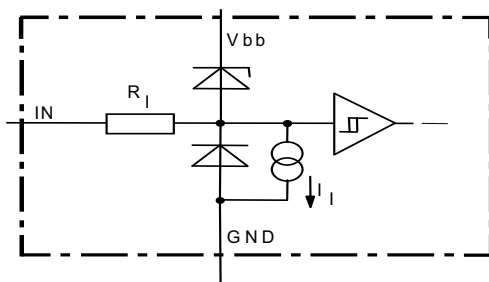
each channel



V_{ON} clamped to 47 V min.

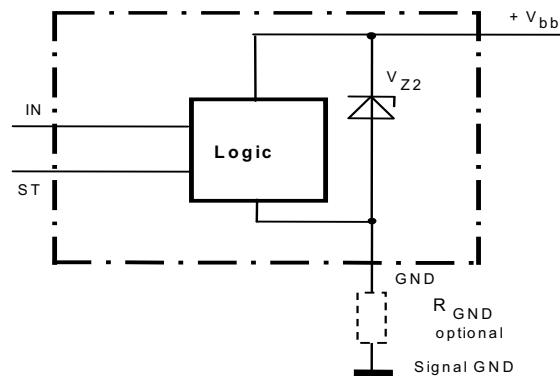
Input circuit (ESD protection)

each channel



The use of ESD zener diodes as voltage clamp at DC conditions is not recommended

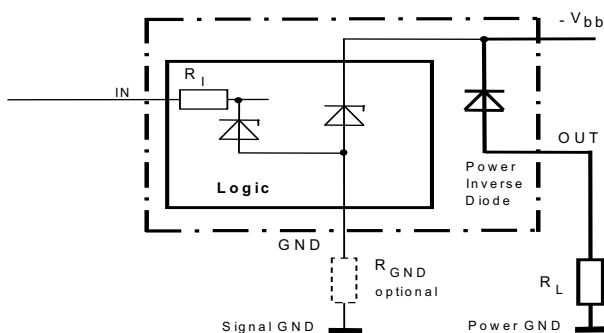
Overvoltage protection of logic part



$V_{Z2}=V_{bb(AZ)}=47\text{ V min.}$,
 $R_I=3\text{ k}\Omega\text{ typ.}$, $R_{GND}=150\Omega$

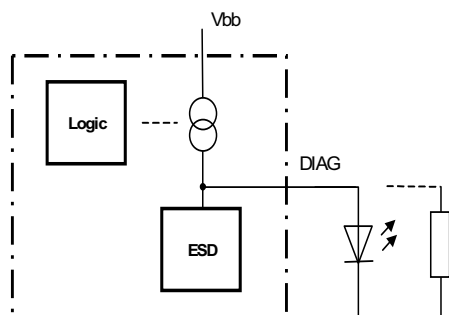
Reverse battery protection

each channel



$R_{GND}=150\Omega$, $R_I=3\text{ k}\Omega\text{ typ.}$,
 Temperature protection is not active during inverse current

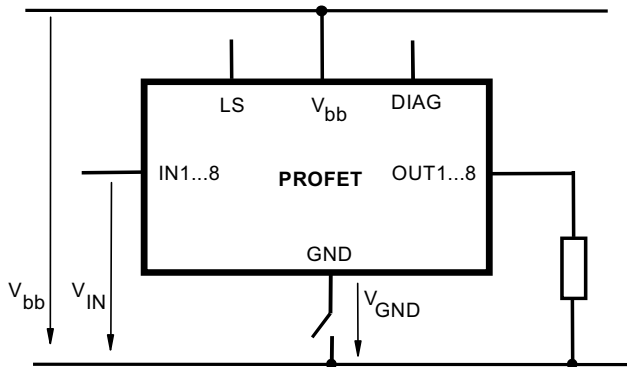
Common diagnostic output



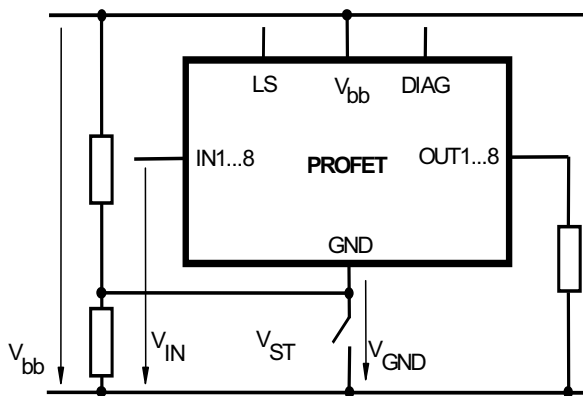
Output current typ. 2 mA

Application Information

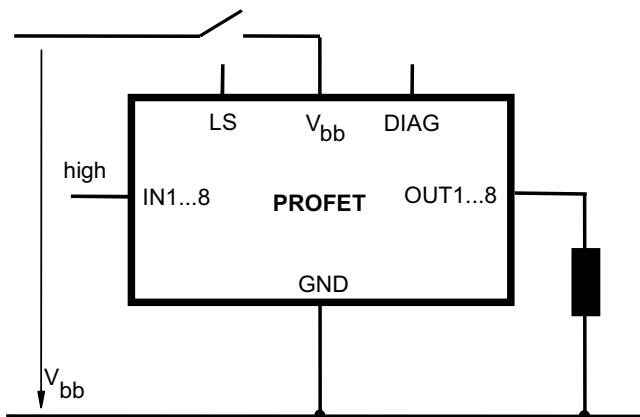
GND disconnect



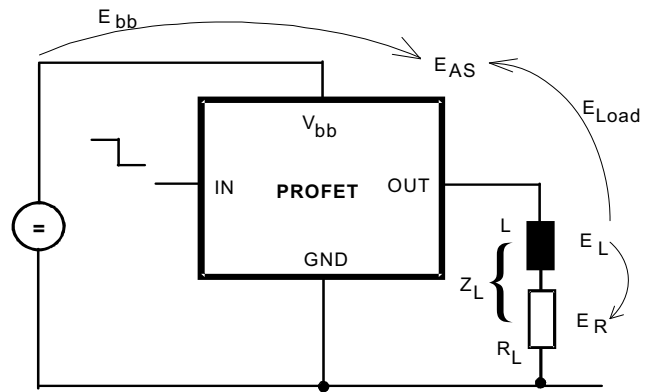
GND disconnect with GND pull up



V_{bb} disconnect with charged inductive load



Inductive Load switch-off energy dissipation, each channel



Energy stored in load inductance: $E_L = \frac{1}{2} * L * I_L^2$

While demagnetizing load inductance,

the energy dissipated in PROFET is

$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} * i_L(t) dt,$$

with an approximate solution for $R_L > 0\Omega$:

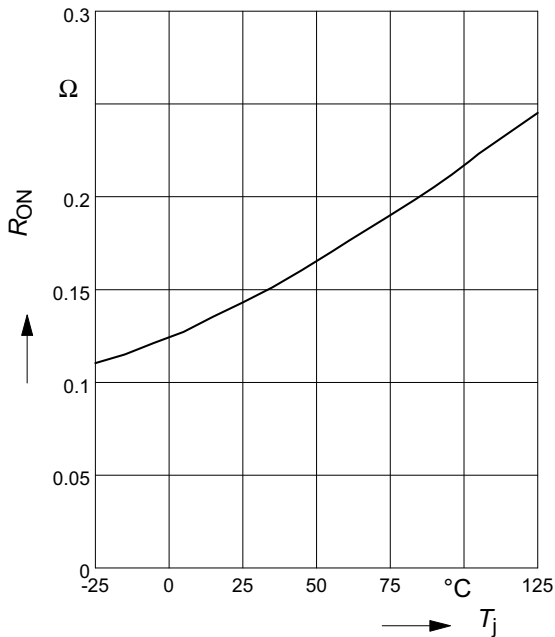
$$E_{AS} = V_{OUT(CL)} * \frac{L}{R_L} * \left[\frac{V_{BB} - V_{OUT(CL)}}{R_L} * \ln \left(1 - \frac{R_L * I_L}{V_{BB} - V_{OUT(CL)}} \right) + I_L \right]$$

Typical Performance Graphs

7 Typical Performance Graphs

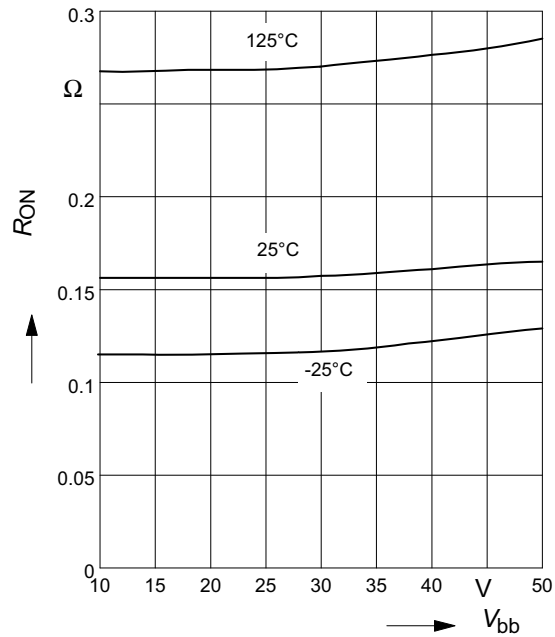
Typ. on-state resistance

$R_{ON} = f(T_j)$; $V_{bb} = 15V$; $V_{in} = \text{high}$



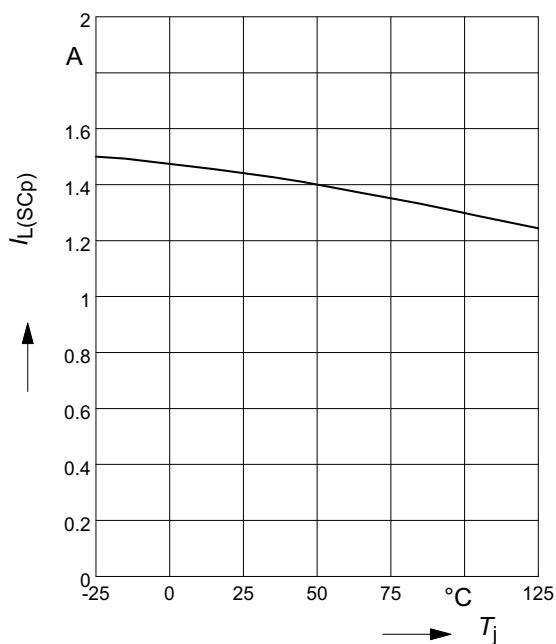
Typ. on-state resistance

$R_{ON} = f(V_{bb})$; $I_L = 0.5A$; $V_{in} = \text{high}$



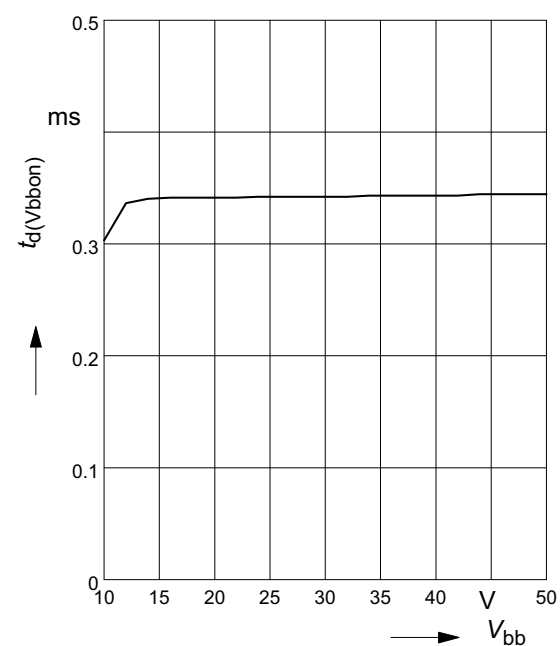
Typ. initial peak short circuit current limit

$I_{L(SCP)} = f(T_j)$; $V_{bb} = 24V$



Typ. input delay time at switch on V_{bb}

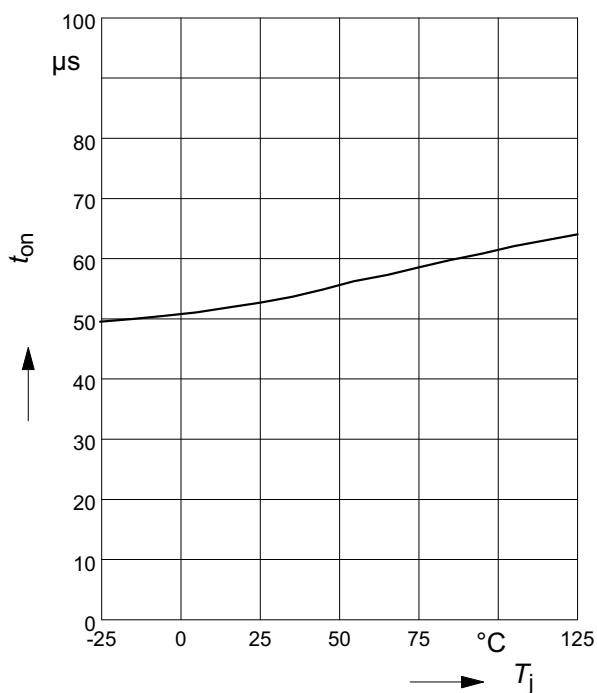
$t_d(V_{bbon}) = f(V_{bb})$; $T_j = -25...125$ °C



Typical Performance Graphs

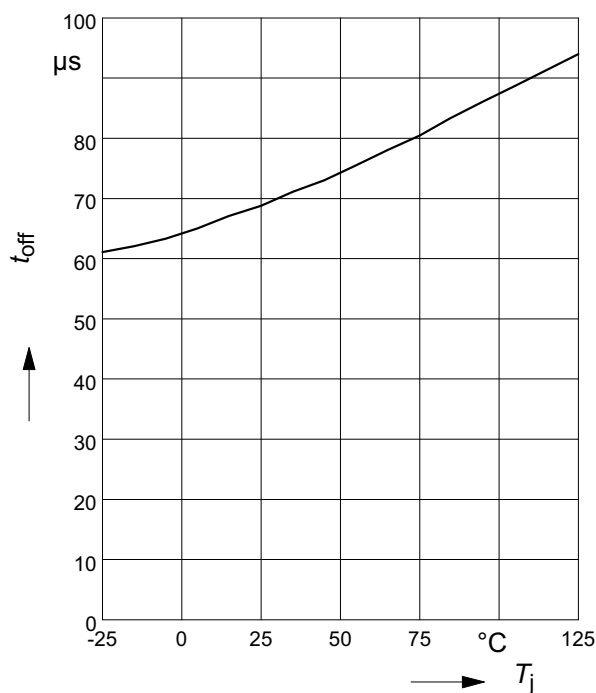
Typ. turn on time

$$t_{on} = f(T_j); R_L = 47\Omega$$



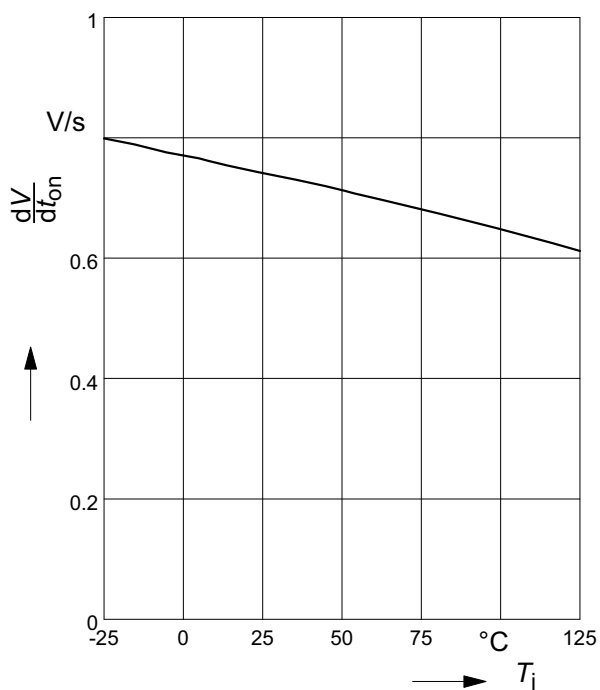
Typ. turn off time

$$t_{off} = f(T_j); R_L = 47\Omega$$



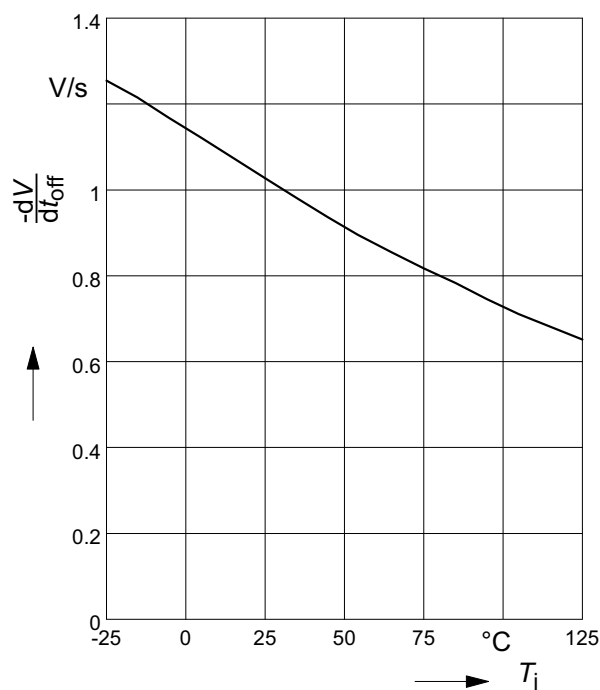
Typ. slew rate on

$$dV/dt_{on} = f(T_j); R_L = 47\Omega, V_{bb} = 15V$$



Typ. slew rate off

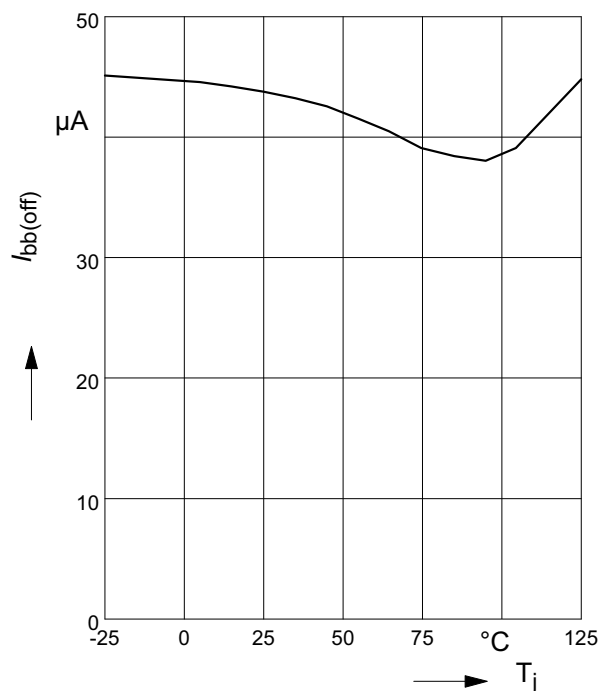
$$-dV/dt_{off} = f(T_j); R_L = 47\Omega, V_{bb} = 15V$$



Typical Performance Graphs

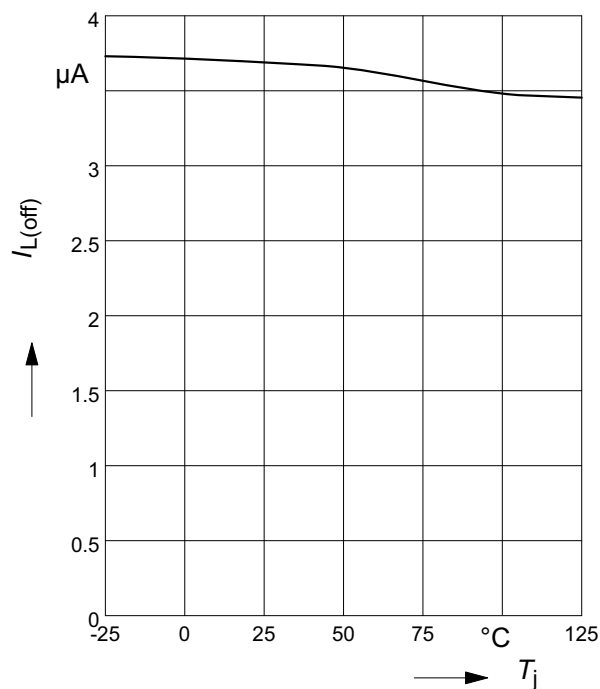
Typ. standby current

$$I_{bb(off)} = f(T_j) ; V_{bb} = 30V ; V_{IN} = \text{low}$$



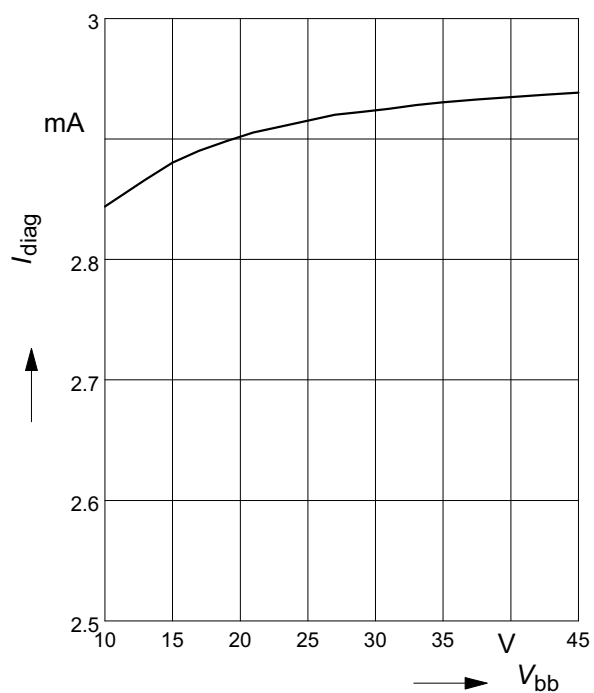
Typ. leakage current

$$I_{L(off)} = f(T_j) ; V_{bb} = 30V ; V_{IN} = \text{low}$$



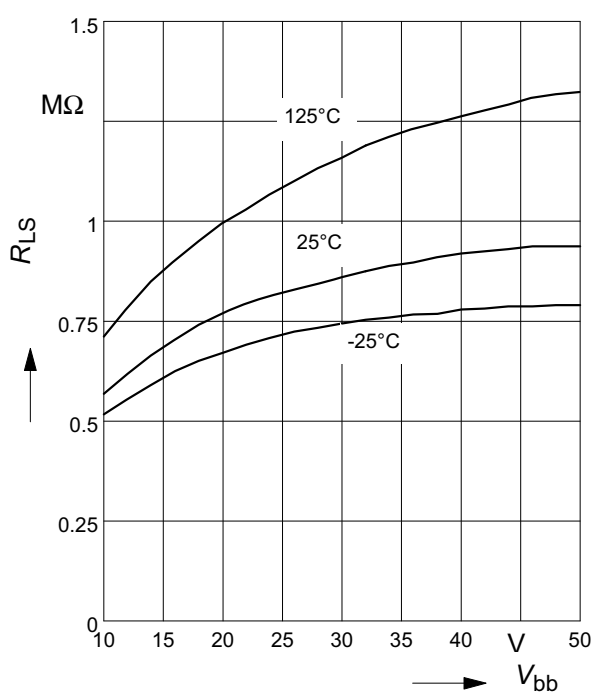
Typ. common diagnostic output current

$$I_{diag} = f(V_{bb}) ; T_j = 135^{\circ}C$$



Typ. internal pull down resistor at LS-pin

$$R_{LS} = f(V_{bb}) ; V_{LS} = V_{bb}$$

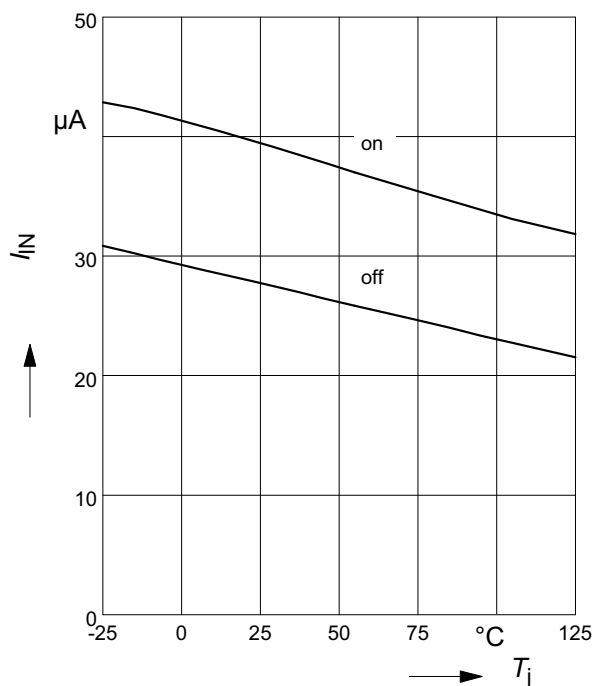


Typical Performance Graphs

Typ. input current @ CMOS level

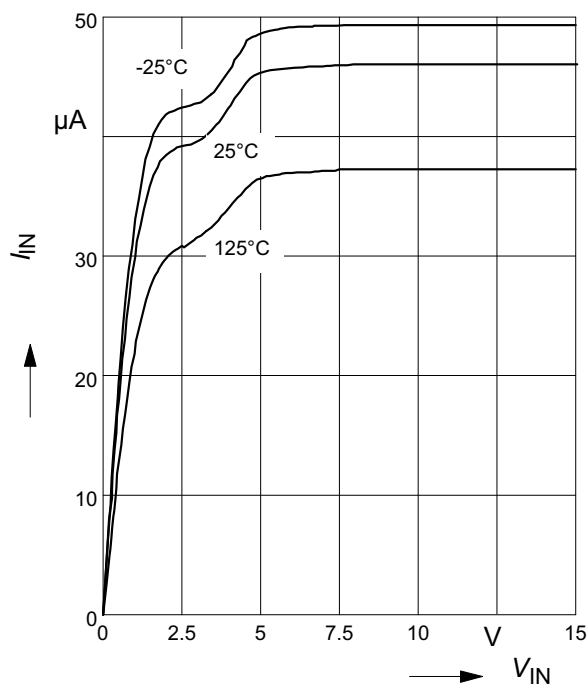
$I_{IN(on/off)} = f(T_j)$; $V_{bb} = 15V$; $V_{IN} = \text{low/high}$

$V_{INlow} \leq 0,8V$; $V_{INhigh} = 2,2V$



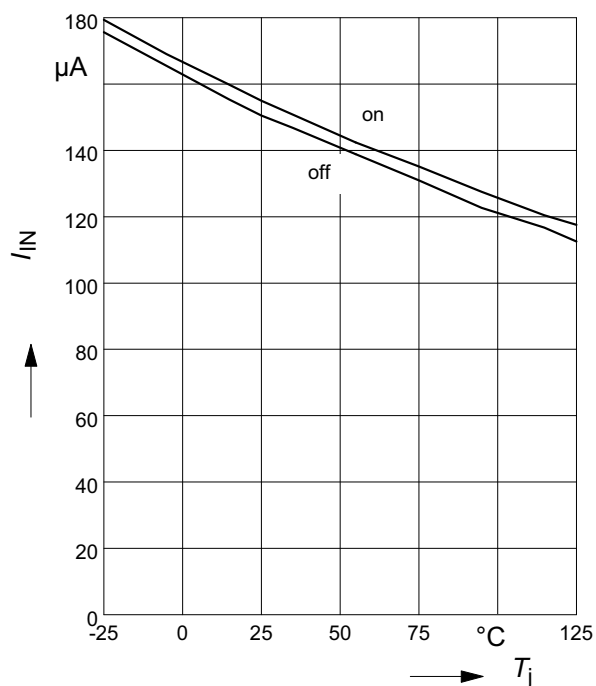
Typ. input current @ CMOS level

$I_{IN} = f(V_{IN})$; $V_{bb} = 15V$



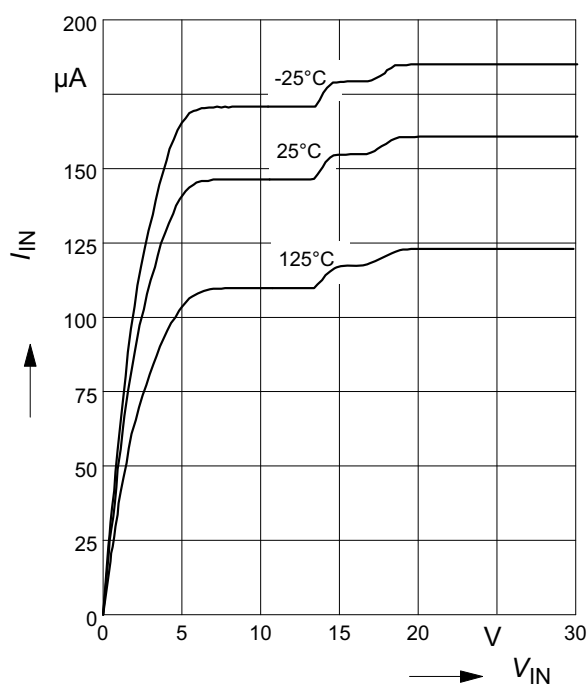
Typ. input current @ V_{bb}/2 level

$I_{IN(on/off)} = f(T_j)$; $V_{bb} = 30V$; $V_{IN} = \text{low/high}$



Typ. input current @ V_{bb}/2 level

$I_{IN} = f(V_{IN})$; $V_{bb} = 30V$

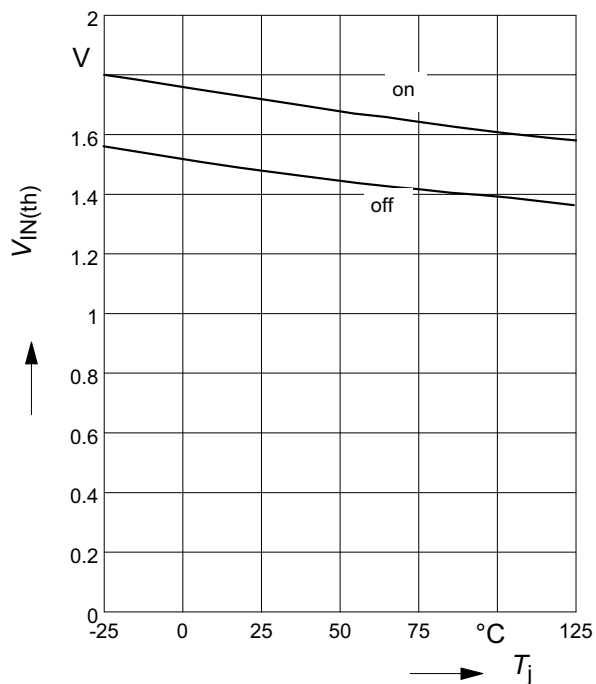


Typical Performance Graphs

Typ. input threshold voltage

@ CMOS level

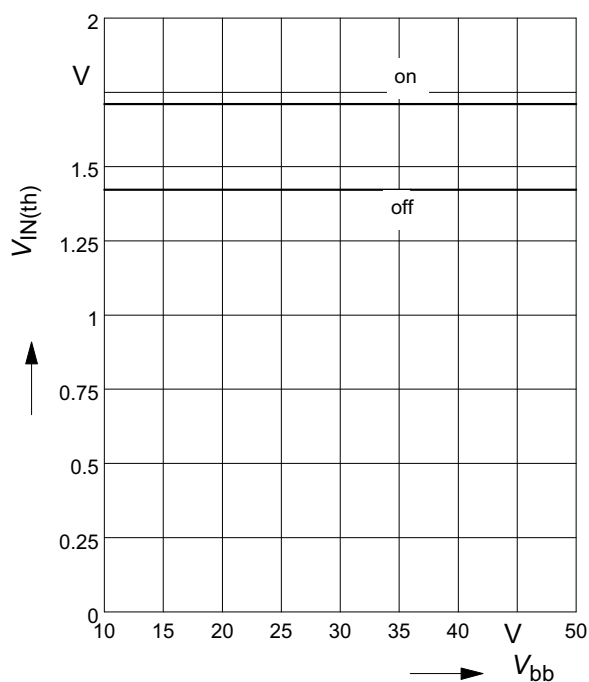
$$V_{IN(th)} = f(T_j) ; V_{bb} = 15V$$



Typ. input threshold voltage

@ CMOS level

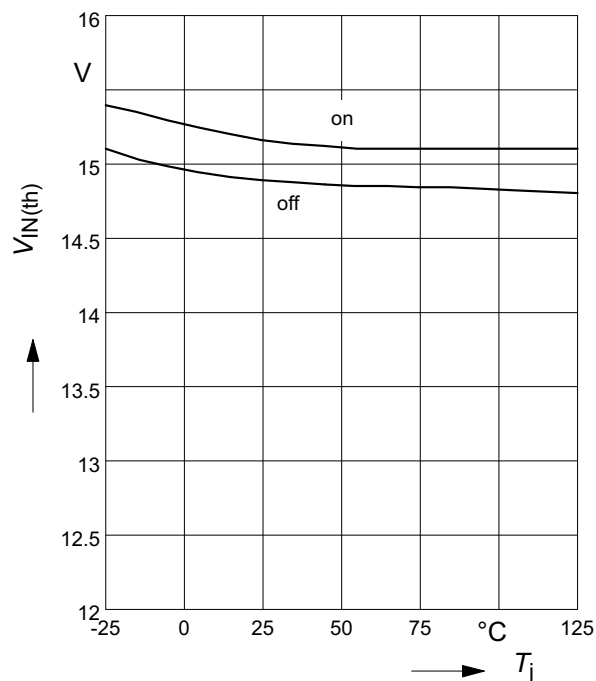
$$V_{IN(th)} = f(V_{bb}) ; T_j = 25^{\circ}C$$



Typ. input threshold voltage

@ $V_{bb}/2$ level

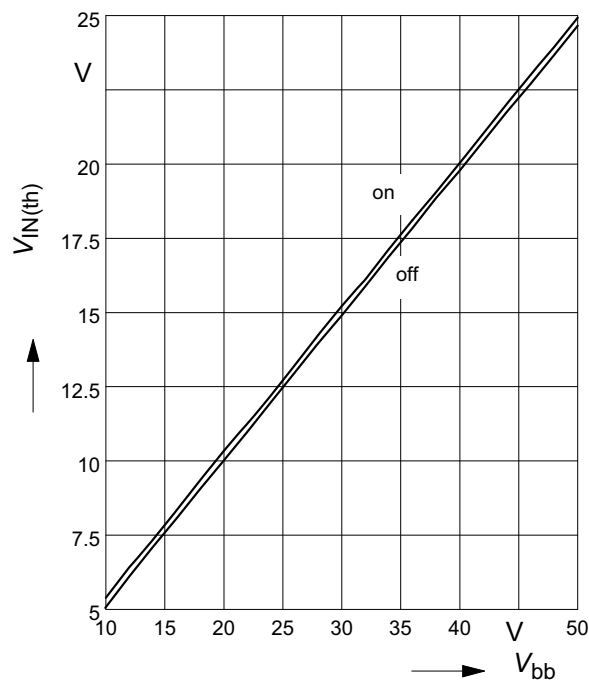
$$V_{IN(th)} = f(T_j) ; V_{bb} = 30V$$



Typ. input threshold voltage

@ $V_{bb}/2$ level: LS-pin connected to V_{bb}

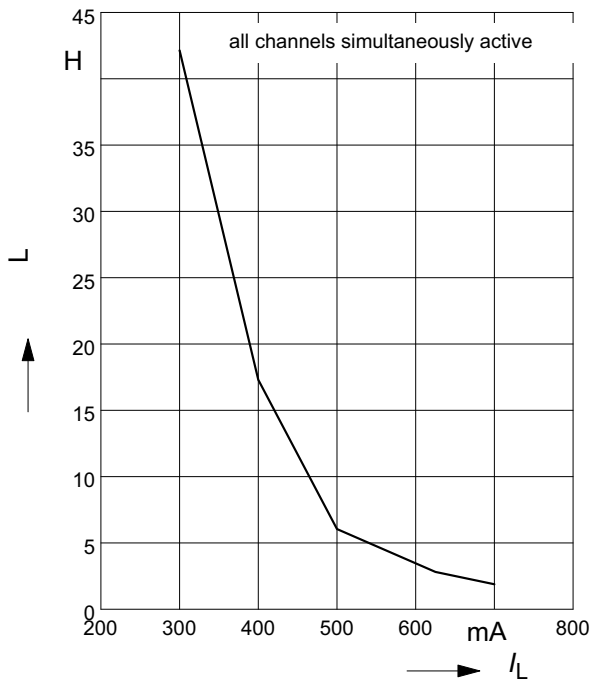
$$V_{IN(th)} = f(V_{bb}) ; T_j = 25^{\circ}C$$



Typical Performance Graphs

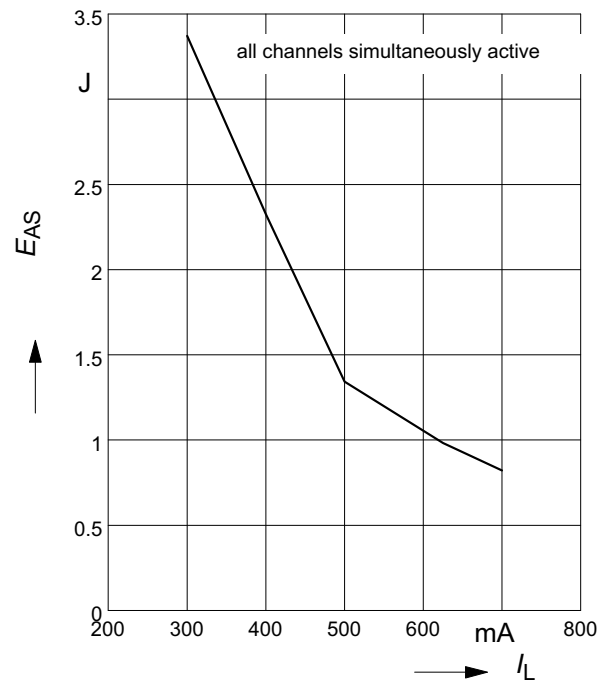
**Maximum allowable load inductance
for a single switch off, calculated**

$L = f(I_L)$; $T_{jstart}=125^{\circ}\text{C}$, $V_{bb}=24\text{V}$, $R_L=0\Omega$



**Maximum allowable inductive switch-off
energy, single pulse**

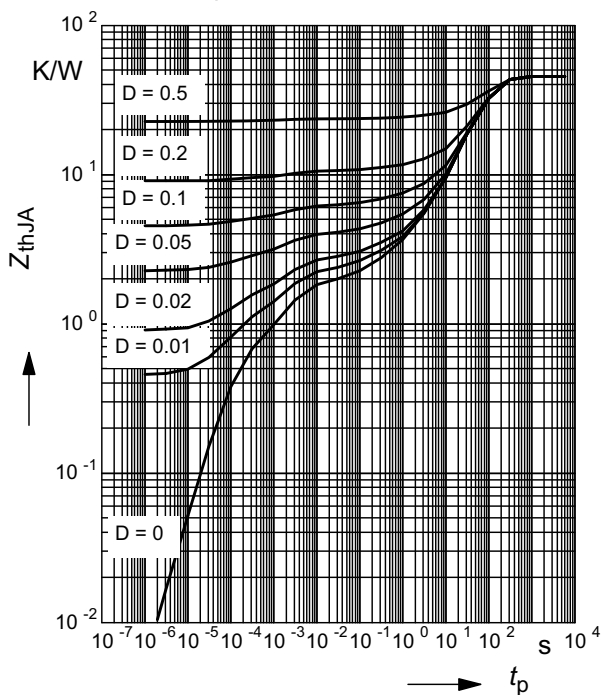
$E_{AS} = f(I_L)$; $T_{jstart} = 125^{\circ}\text{C}$, $V_{bb} = 24\text{V}$



Typ. transient thermal impedance

$Z_{thJA}=f(t_p)$ @ min. footprint

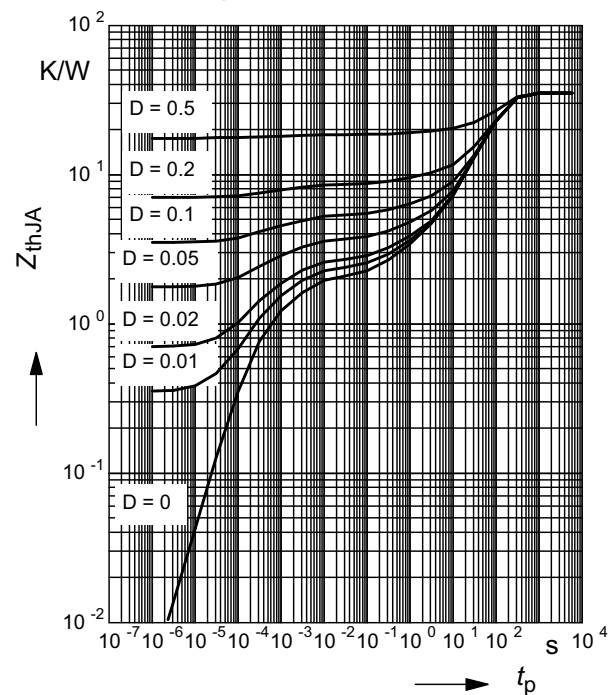
Parameter: $D=t_p/T$



Typ. transient thermal impedance

$Z_{thJA}=f(t_p)$ @ 6cm² heatsink area

Parameter: $D=t_p/T$



Typical Performance Graphs

Timing diagrams

Figure 1a: Vbb turn on:

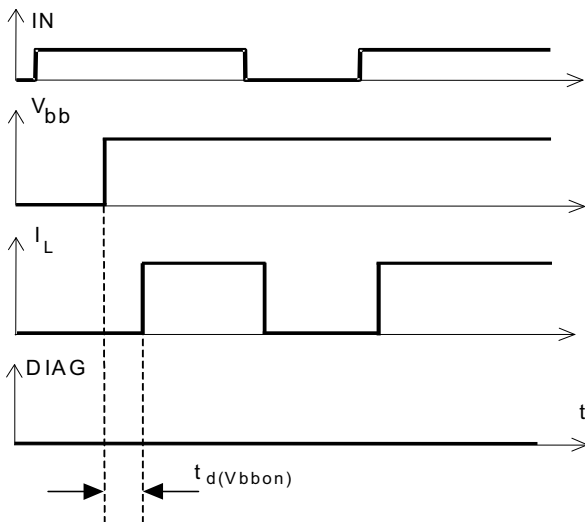


Figure 2b: Switching a lamp

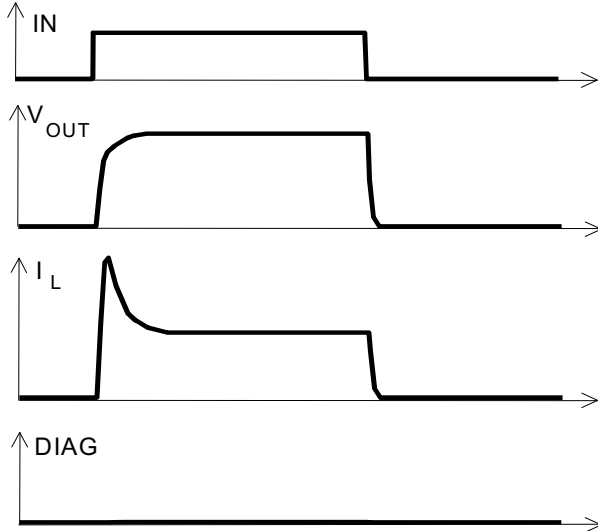


Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition

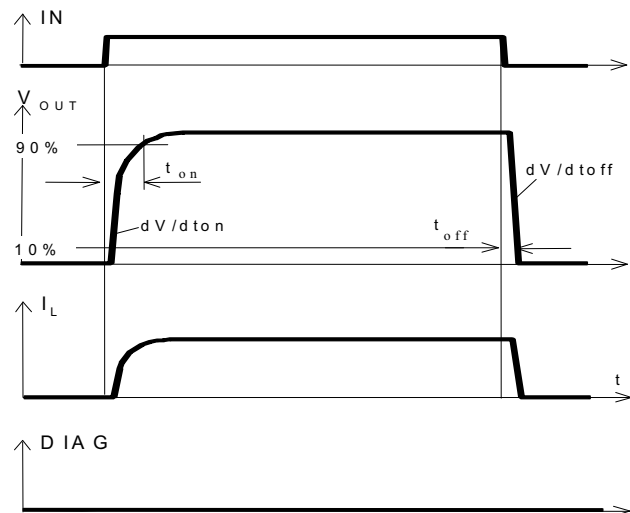
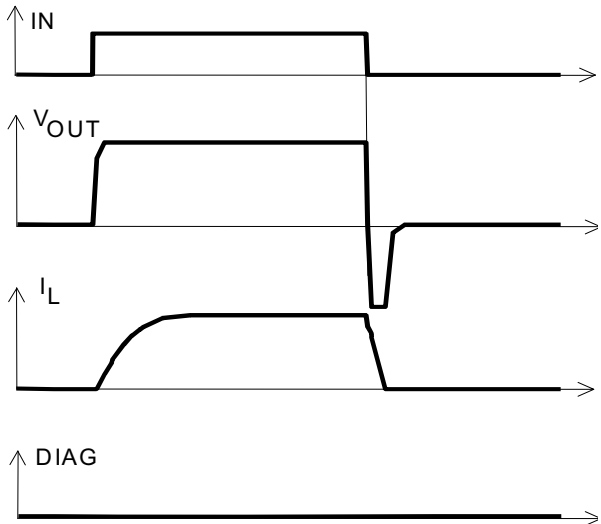
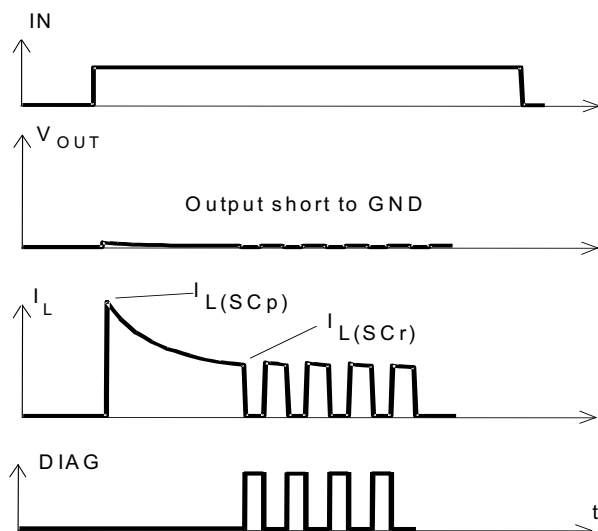


Figure 2c: Switching an inductive load



Typical Performance Graphs

Figure 3a: Turn on into short circuit, shut down by overtemperature, restart by cooling



Heating up of the chip may require several milliseconds, depending on external conditions.

Figure 3b: Short circuit in on-state shut down by overtemperature, restart by cooling

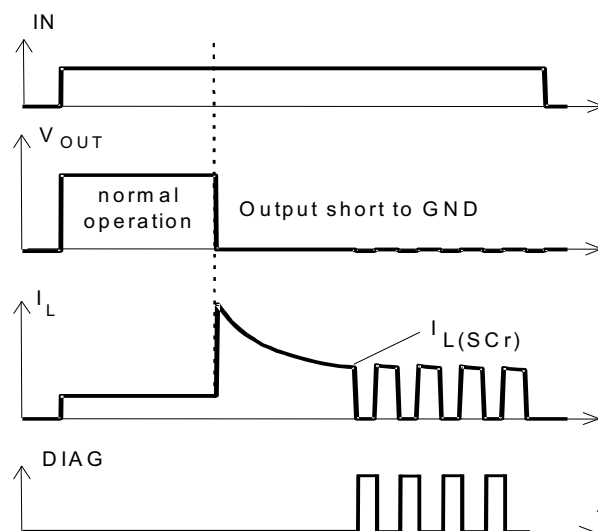


Figure 4: Overtemperature: Reset if $T_j < T_{jt}$

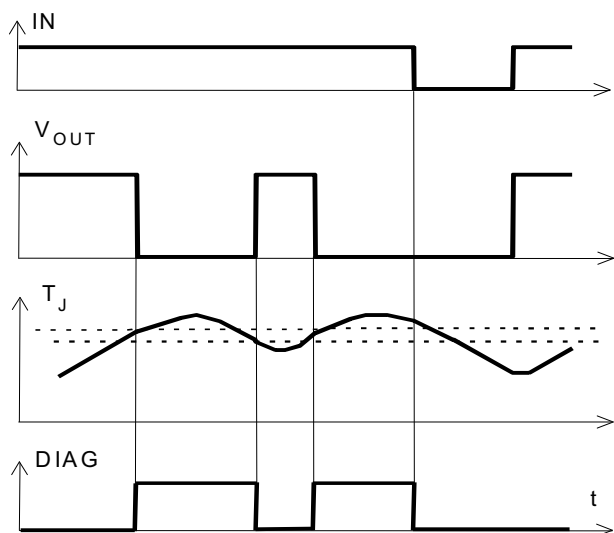
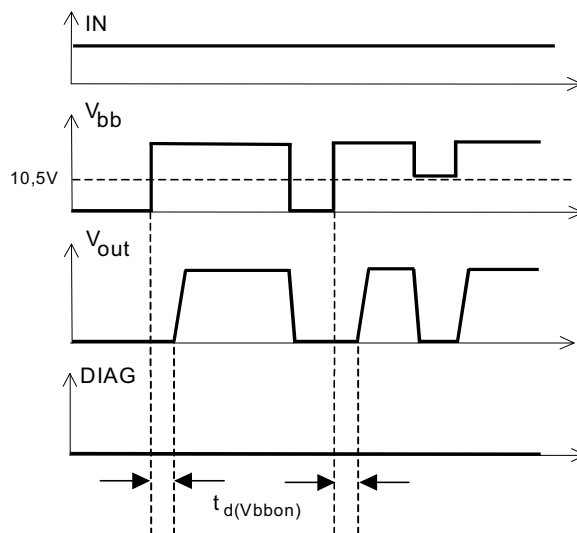


Figure 5: Undervoltage shutdown and restart



8 Package outlines and footprint

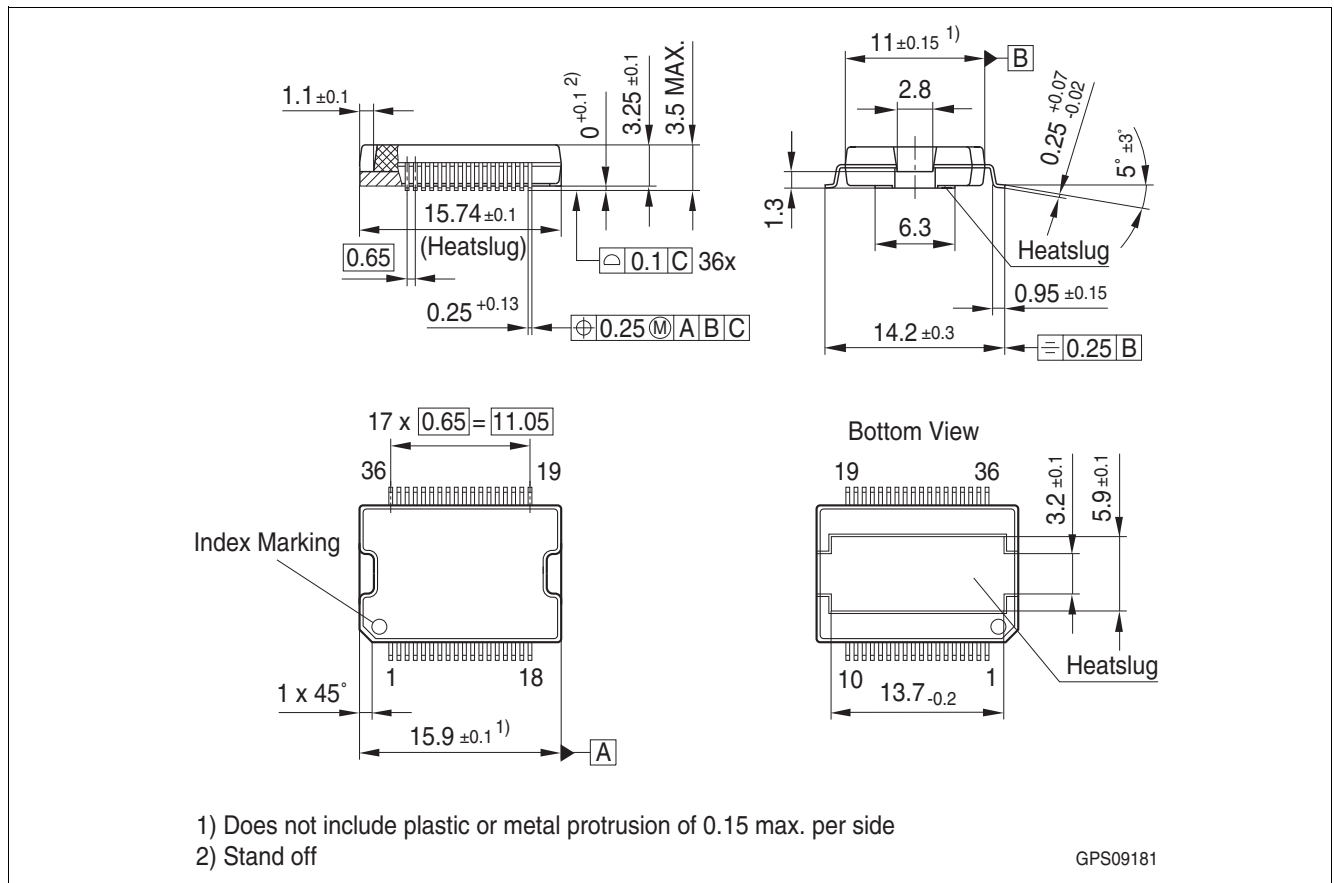


Figure 3 PG-DSO-36-26

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:

<http://www.infineon.com/packages>

Revision History**9 Revision History**

Revision	Date	Changes
1.2	2014-12-10	Update of functional description LS-pin on page 13. Changed wording of the sentence : “Therefore you have either to connect the LS-pin to device GND (state 1) or to supply voltage (State 2).” Changed energy formula New style guide.
1.1	2008-09-30	release all pages: added new Infineon logo Initial version of RoHS-compliant derivate of the ITS4880R Page 1 and 17: added RoHS compliance statement and Green product feature Page 1, 17: Package changed to RoHS compliant version Page 18: added Revision history Page 19: update of disclaimer

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